CHAPTER - 2
LITERATURE SURVEY

The chapter describes the literature survey carried out in understanding the concept of NoC, multistage network, routing schemes, interlink communication and structures to configure a reconfigurable structure. The chapter describes the detailed literature survey based on the different research papers.

2.1 LITERATURE REVIEW

The NoC architecture is an m x n mesh [1] of switches and resources are placed on the slots formed by the switches. It follows a direct layout of the 2D mesh of switches [6, 7] and resources providing physical architectural level design integration. The connection of each switch is with one resource and four neighboring switches, and every resource is connected to one switch. The resources of switches can be a processor core, an FPGA [2], memory, a custom hardware block or any other intellectual property (IP) block, which fits into the available slot and complies with the interface of the NoC [1, 3]. The actual architecture of NoC essentially is the on-chip communication infrastructure comprising the layer relating to data link, physical layer, and the network layer of the Open System Interconnections (OSI) protocol stack model [9]. It can be used to define the concept of a regional hardware unit, which utilizes an area of any
number of resources and switches. The concept is allowed to the NoC, to accommodate large resources such as large memory register banks, FPGA resources areas, or special purpose computation resources such as high performance and multiprocessors. NoC architecture can be differentiated based on network topology, flow control schemes, routing methodology, switching and the techniques applied to ensure quality of service for data transmission.

The topology of a NoC specifies the physical organization of the interconnection network. The topological structure defines switches, nodes and links which are interconnected to each other. Topologies for NoCs [12, 13] can be classified into two broad categories: 1) direct network topologies, in which each node or switch is connected to at least one core IP, and 2) indirect network topologies, where the subset of switches or nodes are not connected to any core IP and performs only network operation. Both direct and indirect topology can be regular like meshes, tori, k-ary n-cubes [15] and fat trees or irregular customized application specific topology. Most NoCs implement regular forms of network topology that can be laid out on a chip surface for a 2D plane, for an example, a k-ary 2 cube (where k is the degree of each dimension and 2 is the number of dimensions) commonly known as grid based topologies. Besides the form, the nature of links adds an additional aspect to the topology. The popular NoC topologies are based on k-ary 2-cube networks, the nature of link are the mesh which uses bidirectional links and torus which uses unidirectional links. For the structures like torus, a folding can be employed to reduce long wires. Millberg et al. has NoC presented the NOSTRUM [15, 16], a folded torus is discarded in
favor of a mesh with the argument that it has longer delays between routing nodes. Generally, mesh topology makes better use of links and their utilization, while tree based topologies are useful for exploiting locality of traffic.

The NoC switching strategy determines how data flows through the routers in the network. NoCs use packet switching as the fundamental transportation mode. Packet switching is a communications paradigm in which packets are routed between nodes over data links shared with other traffic. Packets are queued or buffered in each queue, resulting in variable delay. This is in contrast with the circuit switching, other principal paradigm, which sets up a limited number of constant bit rate and constant delay connections between nodes for their exclusive use for the duration of the communication [5]. In packet switching, instead of establishing a path before sending any data, the packets are transmitted from the source and make their way independently to the receiver that is possibly along different routes and with different delays. There are mainly three kinds of switching schemes [5], store and forward, virtual cut through and wormhole switching.

2.2 FINDINGS OF LITERATURE REVIEW

The following listed papers have discussed, in general, the relevance of NoC architecture, multistage cross bar networks, their routing schemes and testing methodology [17]. It has been suggested by many authors that a NoC structure can follow mesh, tree, ring, torus or hierarchical structures. Each NoC structure has Processing Elements (PEs), which can be reprogrammed based on deflection routing. These papers also explain the layered architecture of NoC, Scalable
Programmable Integrated Network (SPIN) on-chip micro network that defines packets as sequences of 32-bit words, with the packet header fitting in the first word. The network uses a byte in the header to identify the destination address, which allows the network to scale up to \( N \) terminal nodes. In programmable multistage networks each stage can be made programmable and reconfigurable structures. The programmable network enhances the switching capacity of the network and also reduces the blocking probability. Both these advantages have been obtained as the source subscribers are programmed for different possible route to overcome the problem of congestion. The network security has also been an issue, when the data is transferred over long distance [2]. Dual Tone Multi Frequency (DTMF) signaling of multistage networks and Time Division Multiplexing (TDM) techniques are surveyed [41]. The papers discussed here presents different security algorithm. It is found that TACIT network security can be integrated with programmable chip. The detailed survey on these issues is discussed sequentially, with the support of the papers described here.

2.2.1 Andreas Hansson, Kees Goossens and Andrei Radulescu “A Unified Approach to Mapping and Routing on a Network-on-Chip for Both Best Effort and Guaranteed Service Traffic” Hindawi Publishing Corporation VLSI Design Volume 2007, pp (1-16)

In this paper the problem of mapping cores onto any given NoC topology and statically route the communication between these cores is considered. Group presented the UnMappable Read Architecture (UMARS+) algorithm which
integrates the spatial mapping of cores, three resource allocation phases, spatial routing of communication and TDM time slot assignment. As the main contribution they have shown that how the mapping can be fully incorporated in path selection. This allows the formulation of a single consistent objective function that is used throughout all allocation phases. They show how the pruning and the cost metric used in path selection can be extended beyond one channel to capture the nature of virtual circuits. By the incorporation of the traversed path in cost calculations, they derived a metric that reflects how suitable a channel is when used after the channels already traversed. They have shown how a highly flexible turn prohibition algorithm can be used to provide maximum addictiveness in routing of best effort flows. The proposed algorithm is based on the prohibitions on residual resources such that best effort flows can use what is not required by guaranteed service flows. The time complexity of UMARS+ is low and experimental results indicate a run time only 20% higher than that of path selection alone. They applied the algorithm to a Moving Picture Expert Group (MPEG) decoder SoC, improving area 33%, power dissipation 35% and worst-case latency by a factor of four over a traditional waterfall approach.

2.2.2 Hiroaki Morino Thai Thach Bao Nguyen Hoaison Hitoshi Aida Tadao Saito “A Scalable Multistage Packet Switch for Terabit IP Router Based on Deflection Routing and Shortest Path Routing” © 2002 IEEE, IEEE Xplorer, pp (2179-2185)
The paper presents a new scalable multistage packet switch using deflection routing and shortest path routing multistage network. Deflection routing multistage network have advantage of hardware simplicity since switch element has no memory relating to buffers, and variable length packet switching can be easily handled. Moreover, in the methodology proposed by the author, new interconnection method between switch elements, required amount of hardware is reduced compared with conventional switch based on the deflection routing principle. A circuit of 8 x 8 variable length packet switch elements is designed on FPGA, and required amount of hardware to realize a 64 x 64 multistage network is calculated. It is shown that 64 x 64 switches will be implemented within one VLSI chip, and that 10 Tbps is switch is realized by two stage interconnection of the VLSI chips. Multistage network consists of simple deflection routing crossbar switch with no buffer memory inside. Hardware simplicity is the main advantage of the method. Xilinx simulation results show that the proposed method can reduce required amount of hardware of multistage network compared with conventional closed loop shuffle out switch by about 10% under condition that achieving packet loss rate of 5 x 10^{-7}, for 60% offered load in 64 x 64 switch. Circuits of two types of switch elements are floor planed on FPGA device, Xilinx XCV2600E, and they obtained results that needed number of gates for 8 x 8 switch elements is about 27000 gates. For 12 x 8 switch elements, the numbers of logic gates are 40000.
The paper presented a methodology for characterization of NoC switch area and power requirements. The approach, which they have proposed, was based on thorough parameterization on several architectural, deployment, and runtime variables. The area and power models for the Xpipes case study turn out to be very accurate within the limits allowed by the nonidealities of synthesis tools, even when applied to a whole NoC topology with irregular traffic flows. Their experiments show that, at least at the 0.13 μm node, applying the methodology to netlist level devices yields an acceptable approximation of the actual behavior even after placement and routing, but that even greater precision can be achieved, if desired, by applying the same technique at the layout level. They also discussed the tradeoff among accuracy and modeling effort exists, namely, coefficients can be extracted based on a single device instances, by normalization of the synthesis report, or on several of them, by an interpolation process. In their case they have chosen, the rectangular switches to add a smaller amount of information to the training set. For example, when studying the power consumption, a rectangular switch is by design unable to simultaneously feature traffic flows on all of its input and output ports as shown in figure 2.1, and is therefore behaving similarly to a square switch of smaller cardinality. Their preliminary internal testing confirms this property, at least for the Xpipes NoC. Therefore, they simply choose the npi and npo axes for the generation of the
training set, and only include $4 \times 4$, $10 \times 10$, $16 \times 16$, and $20 \times 20$ instances. The work was carried on Xilinx tools and they compared the letlist results.

![4 x 4 pipes with switch architecture](image)

Fig. 2.1 4 x 4 pipes with switch architecture [75]


In this paper the authors proposed a four stage design approach towards securing Vehicular Ad hoc Networks (VANET) architecture with an improved Public Key Infrastructure (PKI) structure. The new structures define by PKI, helps in whilst achieving the security alongside and keeping the users autonomous. The communication between the central certificate authorities is minimized by employing self authorization by the users. It can be attained by self generation of pseudonyms. The scheme discussed here, will help in providing the security to users when not in coverage with the central certificate authority. The
discussed paper also has proposed an efficient way of deploying Certificate Revocation Units (CRL), during revocation scheme which employs car to car forwarding of CRL along with the Road Side Units (RSU). A malicious node is detected only when it is traced back. The Certificate Authority (CA) has to follow back the real holder of a pair of certified pseudonym. Based on the certification issued to CA to work, it is pre determined that the pseudonym and the certificate pair are traceable to the CA. As a node is detected to the CA i.e. to attain the master certificate, it is not denying its authorship later. As soon as the malicious node is detected, the next step for the CA to undertake is to revoke it and distribute this information to every other node. The conclusion of the based is based on that NoC structure is helpful in guiding the mesh topology with the help of their route and address generation scheme to forward the data packets.

2.2.5 Najla Alfaraj, Yang Xu, H. Jonathan Chao “A Practical and Scalable Congestion Control Scheme for High-Performance Multistage Buffered Switches” IEEE 13th international conference on high performance routing and switching 2012, pp (44-52)

The paper explains multistage buffered switches architectures scheme for congestion control which are widely used by the industry such as Cisco, CRS series, Juniper’s ex series and Broadcom’s switch chip sets. They have proposed Hotspot Prevention (HOPE), which is an effective congestion control scheme, used in the 3 stages close NoC. HOPE proactively regulates traffic destined for each output by estimating the number of their backlogged packets in the network
and applying a simple stop and go mechanism to prevent hotspot traffic from jamming the internal links between the stages. In the NoC architecture, the effectiveness of HOPE has motivated the authors to apply it in the multistage buffered switches. The SMs in a multistage buffered switch are separated from each other for a distance up to 100 m, which are different from a NoC, where Switch Modules (SMs) are all on the single chip. The hardware complexity of HOPE can be significantly increased. In the paper, they addressed the implementation challenges when applying HOPE in the 3 stages close network switch. In the particular network case, they proposed a scalable traffic measurement mechanism to approximate the backlogged traffic for each output port by taking advantage of the property of close network that traffic is evenly distributed among central SMs. They have addressed the problem in NoC area, and proposed HOPE [18], an effective and scalable congestion control for the 3 stages close NoC. HOPE monitors and regulates the number of back logged packets in the switch for each output port. The effectiveness and robustness of HOPE have motivated the authors to apply it in the multistage buffered switch. The implementation in NoC was less complicated compared to multistage buffered structure.

The paper explains that Coarse Grained Reconfigurable Architectures (CGRAs) have drawn increasing attention due to their performance and flexibility. Moreover, the applications of them have been restricted to domains based on integer arithmetic since typical CGRAs support only integer arithmetic or logical operations.

The paper introduces approaches to mapping applications onto CGRAs supporting both integer and floating point arithmetic. An optimal formulation is presented using integer linear integrated programming technique. It can present a fast algorithm named Heuristic mapping algorithm. The example of reconfigurable structure is shown in figure 2.2, in which many processing elements are configured in queue as area critical resources. The experiments carried out by them are on randomly generated examples that generate optimal
mapping results using Heuristic algorithm for 97% of the examples within a few seconds. It has been observed similar results for practical examples from multimedia and 3D graphics benchmarks. The developed chips and applications mapped on a CGRA show up to 120 times performance improvement compared to software implementations, helpful in demonstrating the potential for application acceleration on CGRAs supporting floating-point operation. The target architecture consists of a Reconfigurable Computing Module (RCM) [17] for executing loop kernel code segments and a general purpose processor for controlling the RCM, and these units are connected with a shared bus. The RCM used in the platform consists of an array of Processing Elements (PEs), several sets of data memory, and a configuration cache memory. CGRA is containing a 4 × 4 reconfigurable array of PEs. Buses are also shared by the PEs like shared functional units. These two sets of memory are used for double buffering. The configuration cache consists of Cache Elements (CEs), in the form of an array of the same size as the array of PEs, i.e., it has an M number of PEs in a column by N number of PEs in a row array of CEs. Each CE has several layers, so the corresponding PE can be reconfigured independently with different contexts. It is noticed that the area critical resources shared by the PEs in the same row are activated through the individual PEs and, thus, need not be explicitly considered for the modeling of the CEs.
2.2.7 Muhammad Aqeel Wahlah, Kees Goossens, “A test methodology for the non-intrusive online testing of FPGA with hardwired network on chip” Microprocessors and Microsystems, Elsevier (2012), pp (1-18)

In the paper, authors have proposed an online test methodology that uses hardwired network on chip as test access mechanism, helpful to conduct tests on a region wise basis. The methodology used to test on it, exhibits a non-intrusive behaviour that means it does not affect the applications on FPGA regions in terms of network configuration, model, programming, and execution. The methodology used for it, possesses approx, 32 times lower fault detection latency as compared to existing schemes, respectively. They presented an online test methodology for FPGAs applied for Hardwired Network on Chip (HWNOC) as test access mechanism. The online test scheme used by them, ensure the non-intrusive behaviour by: (i) invoking test at application startup time (ii) not allowing disrupted execution for already existing applications, and (iii) not restricting the parallel operations of dynamic reconfiguration and test for multiple applications. The authors analyzed the performance and cost of our test methodology for different Test Configurations Functional Regions (TCFRs) of FPGA architecture. The largest TCFR area was 348 MCRs (5568 CLBs) and the smallest one was with 44 Minimum Configuration Regions (MCRs) (704 CLBs). They were able to detect faults in the largest TCFR in 28.8 ms and at the cost of temporal overhead of 0.021 ms and spatial overhead of 82.4 CLBs.
The article presents a comprehensive performance evaluation of three on-chip communication architectures targeting multimedia applications. The networks considered were compared and contrast the NoC Point to Point (P2P) and bus-based communication architectures in terms of performance, area, and energy consumption. They focused their implementation for bus, P2P, and NoC based implementations of a real time multimedia application for MPEG-2 encoder targeted as FPGA prototype XC2V3000 and actual video clips, instead of simulation and synthetic workloads. The author concluded that the NoC architecture scales very well in terms of performance, area, energy, and design effort, but P2P and bus-based architectures scale poorly on all accounts except for performance and area, respectively. The performance of the NoC based implementation is found very close to the P2P for the same application. Apart from it, the scalability analysis is based on duplicating the bottleneck module in the MPEG 2 design concludes that the performance of the NoC design scales as well as the P2P. Bus based communication and their FPGA implementation scales much more poorly. If NoCs, are analyzed in terms of area, they scales as well as the bus-based implementation. The P2P implementation does not scale well due to the overhead involved in redesigning the interfaces. In terms of space, NoC scales
as well as the bus based implementation. Moreover, the design implementations used for adding new cores to an existing design is much smaller for the NoC case as compared to P2P. The energy consumption of the NoC based architecture and implementation is estimated much smaller than both P2P and bus-based implementations and it scales much quality and better performances with the number of extra modules added to the base design.


The paper explains Scalable Programmable Integrated Network (SPIN) on-chip micro network defines packets as sequences of 32 bits words, with the packet header fitting in the first word. The network uses a byte in the header to identify the destination address, which allows the network to scale up to 256 terminal nodes. The routing information carry packet tagging, and the packet payload can be of variable size. A trailer which does not having data, use a checksum for error detection, terminates every packet. SPIN has a packetization overhead of two words. The payload should be significantly larger than two words to amortize the overhead. On chip networks relate closely to interconnection networks for high performance parallel computers with multiple processors, in which each processor is an individual chip. The networks based on multiprocessor interconnection networks, source and destination nodes are physically closed to each other and have high link reliability. Multiprocessors have traditionally designed using multiprocessor interconnections under stringent
bandwidth and latency constraints to support effective parallelization. The paper explains hybrid network, multistage networks, direct, indirect networks and micro control networks. SoC have arbitration of communication among nodes, reliability and better performance.

2.2.10 Vasilis F. Pavlidis, Eby G. Friedman “3D Topologies for Networks-on-Chip” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 15, No. 10, October 2007 pp (1081-1091)

The paper explains the chip integration of 2D and 3D NoC topological structures. NoC Integration in the third dimension introduces a variety of topological structures choices for configurable NoCs. In 3D NoC, each Processing Elements (PE) is on a single axis but possibly different physical plane (3D IC–2D NoC). By the chip integration point of view, a PE can be implemented on only one of the physical planes of the system. Therefore, each 3D NoC contains PEs on every physical planes such that the total number of nodes is \( N = n_1 \times n_2 \times n_3 \), where \( n_1, n_2, n_3 \) are the number of nodes in X, Y and Z directions. The different configurations of 2D and 3D NoC are shown in figure 2.3. A 3D NoC topology is proposed in figure 2.3(c), in which exists one physical plane. Each PE can be integrated in multiple planes, as (2D IC-3D NoC). Based on this integration, It is possible to form a hybrid 3D NoC. In such a NoC system, both the interconnect network and the PEs can span more than one physical plane of the stack (3D IC - 3D NoC). The paper emphasized on the research work towards latency expressions for each of the NoC topologies, with the assumption of a zero load.
model. The speed and power consumption of 3D NoC are compared to that of 2D NoC, their physical constraints, such as the maximum number of planes that can be vertically stacked and the asymmetry between the horizontal and vertical communication channels of the network. An analysis is done on their performance and analytic model for the zero load latency of individual network that considers the effects of the topology on the performance of 3D NoC is also developed. 3D - 3D network provides zero latency but for crossbar structure, 2D - 3D NoC structure can be preferred for a larger network where power and delay are major constraints.

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Fig. 2.3 Various NoC topologies [98] (not to scale) (a) 2D IC–2D NoC. (b) 2D IC–3D NoC. (c) 3D IC–2D NoC. (d) 3D IC–3D NoC.

2.2.11 Mike Santarini “FPGA Command Centre Stage in Next Gen Wired Networks” XCell Journal Today, Vol.1 issue 67, (2009), pp (10-14)
The paper explains two types of wired network, one for computing and the second for telecommunications. Wired networks have been separate, their own set of unique protocols, bandwidth requirements routing equipment and rate of bandwidth growth. In telecom industry bandwidth requirement has increased four times (2.5 Gbps to 10 Gbps), and now moving to 40 Gbps). On the other hand, computer networking has done the job in leaps of 10x (100M, 10G, and 100 G). Therefore, a distinguished engineer Goron Brebner from Xilinx noted that during the last wired network retooling a few years ago, a convergence of sorts took place at 10 Gbps. The physical signaling for Ethernet has been converged with signaling for telecom as both network types independently increased their top bandwidth rates. In telecommunication, a line card is a combination of a series of dedicated Network Processor Units (NPUs), a CPU and a number of the highest speed FPGAs available. As a packet arrives at a line card, an FPGA processes the raw data into formats that a given router can read. The NPUs are coordinated by the processor to read and route data, while the FPGAs facilitate some of the communication between the CPU and the NPUs. Future generation wired networks will be transferring internet data, voice, and video simultaneously with the integration of all these into IC package. In June 2008, telecommunications giant Comcast Corp. announced, it had successfully completed a 100 Giga bit Ethernet (GE) technology test over its existing backbone infrastructure between Philadelphia and McLean, Va., using the industry’s first 100GE router interfaces. The system used the same High Speed Ethernet IP Core (HSEC) running on a Virtex-5 Full Duplex Transreceiver (FXT) FPGA board, which is supported by
the Virtex-5 platform today. Virtex-5 TXT XC5VTX240T device contains 37,440 logic slices with a total of 239,616 logic cells. The Xilinx FPGA electrically transmitted all ten signals to ten 10 Gbps (Small Form Pluggable Factor) XFP optical transceivers, which converted the signals into the optical domain.


The paper presents the use of FPGAs in the implementation of both analog and digital modulation that includes Amplitude Modulation (AM), Frequency Modulation (FM), Phase Modulation (PM), Pulse Code Modulation (PCM), Pulse Width Modulation (PWM), Pulse Position Modulation (PPM), Pulse Amplitude Modulation (PAM), Delta Modulation (DM), Amplitude Shift Keying (ASK), Frequency Shift Keying (FSK), Phase Shift Keying (PSK), Time Division Multiplexing (TDM) and different encoding techniques like Non Return to Zero (NRZ) line code, NRZ mark line code, NRZ inversion line code, Unipolar NRZ line code, bipolar NRZ line code, alternate mark inversion line code, and Manchester line code. Moreover, the designing of FPGA can be done to emulate a particular device like an oscilloscope and a function generator. The paper describes the capability of an FPGA to internally generate a low frequency input signal and through the use of a Video Graphics Array (VGA) port, and it is
capable to display the signals in an output device. The paper focuses that the use of FPGAs is not limited to the aforementioned applications because of its reconfigurability and reprogrammability.


The paper demonstrated design and construction of microcontroller based telephone exchange system, connection with Programmable Interface Controller (PIC) 16F877A and DTMF MT8870D. In telephone system, PIC16F877 microcontroller is used to control the call processing. When call is processed, different tones are generated which are dial tone, busy tone and ring tones. The paper demonstrates the eight line telephone systems with full signaling and switching functions similar to those of the central office systems. The eight telephones are connected to the switching devices and common line. In microcontroller system, PIC16F877A microcontroller is utilized to control tone, ring relay and on/off-hook switch when the telephone is used. In the designed system there is tone generator, which is used to get dial tone, ring tone and busy tones. Ringing is generated at the receiving end of the phone being called. Ring relay is used to get tone and ring processes. DTMF signaling technique is based on basis for voice communication control. Each number consists of a combination of two frequencies. DTMF decoder converts the DTMF tones to the binary numbers and sends to the microcontroller. In the signaling and switching
operations, transistors and relays are used to switch audio signals and control signals and to decode the DTMF signals. These switches are controlled by powerful software procedures to be implemented.


The authors have applied the new approach to design high performance Hybrid Telephone Switching System (HTSS) using combination of stored program control (SPC) electronic switching system and VLSI technology. They proposed to separate total digital processor card circuit around processor into two parts. One is service handling circuit (SHC) and another is call handling circuit (CHC). For the good performance of the system, it is very important to increase the call handling speed of system. The speed of the system is increased with the use of SHC and CHC because CHC is designed to work in concurrent manner to handle individual calls of subscribers and SHC helps CHC while any service/facility is to be provided. SHC is having all features of SPC with removed call handling operations. In a general way, each line card includes driver circuit of eight lines. In the same time, different functions are incorporated on the line cards and those perform many switching functions by themselves. The sub unit CHC performs all those functions. Whenever an electronic circuit is designed, the size of the circuit is the very important factor. The authors were able to reduce CHC in
to single IC. Therefore, it is possible to use reduced processor card that could be placed in any corner of line cards. They designed CHC to work with eight lines so that it can be placed with each line card. The drive circuit is carried out using junction card for trunk lines and switching matrix establishes the connection between calling subscriber and called subscriber or between junction line and calling line. The operations relating to call handling are handled by concurrent operations using CPLD and complicated and sequential operations like services handling are handled by Microcontroller/ Microprocessor Systems (MPMC). VHDL codes are designed and tested for different test cases on call handling operations and verified using test benches are designed to act as MPMC for the testing of services like Do Not Disturb (DND), Outgoing Bar (OGB), Call Forwarding (CF), and STD Bar (STDB) facilities.


In the article, the authors have presented an overview for NoCs using a complete NoC synthesis flow, design, and a detailed scalability analysis of different NoC implementations for the latest nanometer scale technology nodes. They presented NoC based solutions for the on chip interconnects of Multiprocessor System On Chip (MPSoCs) that illustrate the benefits of competitive application specific NoCs with respect to more regular NoC
topologies regarding performance, power and area. Emerging consumer applications demand a very high level of performance in the next generation of embedded devices. Therefore, a new techniques and interconnection mechanisms that can provide solutions for an efficient design of the system complex for the coming embedded architectures are greatly needed. The impact of the target frequency of operation on the area and energy consumption of an example 5 x 5 switch obtained from layout level estimates for 130 nm is presented, and energy values (in power MHz) instead of the total power, so that the inherent increase in power consumption due to an increase in frequency. The paper emphasizes the use of 3D NoC instead of 2D NoC in terms of scalability and reliability, their structure and routing. It is completely based on the review of NoC topological structures.

2.2.16 Jason Cong, Yuhui Huang, and Bo Yuan “A Tree-Based Topology Synthesis for On-Chip Network” Computer Science Department University of California, Los Angeles Los Angeles, USA, IEEE Conference proceedings, (2011)pp (650-658)

The Network on Chip (NoC) interconnect network of future multi-processor system on chip (MPSoC) needs to be efficient in terms of energy and delay. The custom on chip network, which targets a given application, has proved to be more efficient than the regular structure on-chip network design in. The reason is that the communication requirement for each data flow is available in the design time, so the packet latency and power consumption are predictable
once the links of networks are determined. The problem of topology synthesis is to determine the number of routers, the location of newly added routers, and the connectivity between them. Power consumption and packet latency are two trade-off factors for any Application Specific Integrated Circuit (ASIC) design which are met in the research. The paper has focused more on tree topological NoC implementation in Hardware Description Language (HDL) environment.


The paper focuses about a Multistage Interconnection Network (MIN), which is composed of several stages of switch elements by which any network input port can be connected to any output port. In the paper, optical MIN is represented and its capability.

It a very important class of interconnecting schemes used for constructing optical interconnections for communication networks and multiprocessor systems. Hybrid structure is used to represent the most commonly implementation approach with guided wave technology. In the structure main basic Switching Element (SE) in hybrid optical MINs, which is also called directional coupler and is typically fabricated on Titanium Diffused Lithium Niobate (Ti:LiNbO3). MIN architecture has multicast capability, used in telecommunication switching which is constructed utilizing a modularization approach for fixed exchange pattern. It
consists of an input module, two Point to Point (PTP) modules, and one or more Multicast/Broadcast (M/B) and an output module as shown in figure 2.4.

![Diagram of N x N multistage network](image)

Fig. 2.4 N x N multistage network [35]

The input signal is taken by input to PTP and M/B modules, which are independent to each other. PTP can follow any MIN architecture and M/B provides multicast functions. The comparison is also carried out to indicate that this new architecture with Dilated Benes PTP module has much better performance in terms of system Signal to Noise Ratio (SNR), signal attenuation, the number of switch elements of point-to-point connections than two current multicast MIN architectures, PS/AC and Jajszczyk’s networks.
The paper focuses on fault tolerance design of the communication links in NoC architecture. They proposed link structures that have properties for tolerating efficiently transient, intermittent, and permanent errors. Transient errors can be realized using Hamming coding technique methods and interleaving for error detection and Automatic Repeat Query (ARQ) as the recovery method. Two approaches have been introduced to tackle the intermittent and permanent errors. Time redundancy can be utilized using split transmission approach, while the other structure, introduced are using spare wires, is a hardware redundancy approach. Network communication in the links was based on asynchronous 2-phase signaling and the control signals for ARQ and reconfiguration were incorporated into these control signals. The control lines are used to control the functionality of the network and protected using triple modular redundancy. The developed designs compared against reference designs and simulated. From the simulation results, it has been shown that the performance of NoC decrease when comparing to a design with ARQ, but no reconfiguration structure is larger for the split transmission design than for the spare wire design. Split transmission has latency 31%, throughput 25% and spare wire has latency 15% and throughput 10%. Moreover, the area overhead is larger for the spare wire design (105%) as for the split transmission design (75%).
2.2.19 Wen-Chung Tsai, Ying-Cherng Lan, Yu-Hen Hu, and Sao-Jie Chen

The paper focuses the layered protocol architecture of NoC. The routing scheme of 5 x 5 crossbars NoC is also discussed in the paper. The typical architecture of a mesh NoC is shown in figure 2.5 which is a combination of multiple segments of wires, Network Interfaces (NI), and routers (R). Each interface can have either source IP or destination IP. The NoC function can be performed into several layers: application layer, transport layer, network layer, data link layer, and physical layers.

![Fig.2.5 Typical NoC architecture in a mesh topology [99]](image_url)

For every NoC router, it should contain both software and hardware implementations to support functionality of these layers. In the end of the paper,
they proposed a novel Bidirectional Channel NoC (BiNoC) backbone architecture. It can be easily integrated into most conventional NoC designs and successfully improve the NoC performance with a reasonable cost and power.

2.2.20 Krishnan Srinivasan, “OCP-IP Network-on-chip benchmarking workgroup Erno Salminen”, Tampere University of Technology Sonics Inc. Zhonghai Lu, Royal Institute of Technology, December 2010, pp (1-5)

Multiprocessor System on Chip (MPSoC) devices integrate multiple processing elements, memories, peripherals, and off chip interfaces into a single silicon chip. It allows higher performance with reasonable power consumption, which is critical in mobile devices but also in many other embedded systems. The highest demand is of efficient parallel processing for the interconnect network that is utilized inside the chip; this is also called a Network on Chip (NoC). The practical implementation and adoption of the NoC design paradigm faces multiple unresolved issues related to design methodology/technology and analysis of architectures, which are helpful in test strategies and dedicated Computer Aided Design (CAD) tools. Benchmarking has been a long tradition in CPU and compiler design. To advance and accelerate the state of the art of the NoC paradigm research and development, the community is in the need of widely available reference benchmarks. Open Core Protocol International Partnership (OCP-IP) is dedicated to proliferating a common standard for intellectual property (IP) core interfaces, or Sockets, that facilitate “plug and play” System on Chip (SoC) design. Implementing complex SoC design more efficient
for the widest audience services, OCP-IP provides the tools and services to its members that are necessary for convenient maintenance, implementation and support of the standard OCP socket interface. There are several workgroups each concentrating on a certain topic, used as socket specification, assembling, system level design, co-design, debug, and NoC benchmarking. The article described in the paper presents the goals and deliverables provided by the NoC benchmarking workgroup. The NoC implementation and OCP interface using pipelined structure and parallel processing is an extensive research in the implantation of NoC benchmarking.

2.2.21 Aurel A. Lazar, “Programming Telecommunication Networks” IEEE Network, September 1997, pp (8-19)

In the paper authors have discussed the realization of an open programmable networking environment based on a new service architecture for advanced telecommunication services that overcomes the limitations of the existing networks. The paper investigating a model will help to clarify some of the pertinent issues confronting the telecommunications service industry today as it comes of age. The paper focuses the programmable switch implementation of telecommunication network. They address some of the important QoS, performance, scalability, and implementation issues, fully aware that our work has opened new vistas that call for additional research. The paper exploits the advantages offered by IP and ATM technologies without necessarily suffering their shortcomings. The need for investigating scaling issues through the
emulation of complex service scenarios arising in large scale broadband networks is much focused in the research paper. The research paper is a start in the era of programmable telecommunication network and their reconfigurable structures.


The paper presents novel high speed architecture method for the hardware implementation of the Advanced Encryption Standard (AES) algorithm used for network security. The paper is an extensive research towards sub pipelined architecture in network security. In order to explore the advantage of sub pipelining further, data is implemented by a combinational logic to avoid the unbreakable delay of Look up Tables (LUTs) in the traditional designs. Encryptor and decryptor both can enjoy of 128 bits of block size at encryption and decryption end respectively, but the key size is possible to keep up to 128, 192 and 256 bits respectively. Using the proposed methodology, a fully sub pipelined encryptor with 7 sub stages in each round unit can achieve a throughput of 21.56 Gbps on a Xilinx XCV1000 e-8 Bg 560 device in non feedback modes, which is faster and is 79% more efficient in terms of equivalent throughput slice than the fastest previous FPGA implementation known to date.

2.2.23 Prosanta Gope, Ashwani Sharma Ajit Singh Nikhil Pahwa “An Efficient Cryptographic Approach for Secure Policy Based Routing (TACIT
High performance internetworks need the freedom to implement packet forwarding and routing to their own defined policies in a way that goes beyond traditional routing protocol concerns, but there are some administrative issues dictate the traffic be routed through specific path. With the help of policy based routing users can implement policies that selectively cause packets to take different paths. In a staged network it is much needed to route secured data towards destination. Therefore, the secured policy routing methods are applied. The paper focuses compares the different methods available for network security such as DES, Triple DES, AES, Blowfish, RC4, Modes, X-Modes, but these methods are limited to block size and key size. Maximum key size is supported by AES algorithm of 256 bits. In the paper, authors have proposed a new security algorithm, TACIT encryption and decryption, which can be applicable to any network. The greatest advantage of the algorithm is that it can have ‘n’ bits block size and ‘n’ bits key size. The hardware chip implementation of the TACIT network security is the future work proposed by the authors and it can provide the best results if key size is considered greater than the block size. The algorithm has been tested on the different text files. It can be implemented in C, C++, C# and Java programming languages.

2.2.24 Nikos Sklavos, Alexabdros Papakonstinou, Spyros Theoharis Odysseas Koufopavlou, “Low-power Implementation of an Encryption/Decryption
The paper has focused, a low power VLSI block encryption system design and implementation. The choice of International Data Encryption Algorithm (IDEA) as the encryption/decryption algorithm ensures the strength of the data encryption operation. The paper presented the two implementations of the system which are synchronous and asynchronous. The only known fast single chip implementation is synchronous design. The synchronous chip has a power consumption of the 1.25 W, while the chip designed by the authors for synchronous version has a power consumption of 58 mW and our asynchronous 41.25 mW in the worst cases of operation. Moreover, their synchronous design has low power dissipation, and the asynchronous design has significantly very low power consumption. Apart from it, with the second implementation of asynchronous design of the encryption/decryption system the total power dissipation is decreased at about 20–40 % in percentage units. The same integrated circuit can be applied as a very fast and low power encryption/decryption device in high speed networks such as multistage telecommunication networks or 2D and 3D NoC.

2.2.25 Nikos Chrysos, Lydia Y. Chen, Cyriel Minkenberg, Christoforos Kachris and Manolis Katevenis “End-to-end congestion management for non-blocking multistage switching fabrics” ACM digital Library, (2010), pp (1-2)
Scalable network routers and high performance computer interconnects are encountered as packet switched networks. As these networks scale to larger port counts, and their utilization increases, helpful in congestion management becomes indispensable. There are some technology constraints rule out monolithic buffer less switches with centralized schedulers, and proposed buffered multistage switching fabrics with distributed control. The controlling of multistage network is discussed in the paper. There is an arbiter, located in central scheduling unit and it can be distributed across switches and fibers. The network was considered of 64 x 64 size, three stage network. The authors depicted the average delay of packets = 2.5 x bursty arrival time and each request can be granted under 128 segments of Virtual Output Queue (VOQ).

2.3 RESEARCH GAPS

As seen from the literature survey that the various articles have presented the concept of multistage networks, NoC structures, routing schemes. It also describes HOPE, VANET, UMARS+, Xpipes NoC, 2D-3D NoC switching, buffering techniques and scalable structures. In multistage networks there is the research gap in the implementation of programmable switch. The research can be focused in the implementation of programmable reconfigurable structure with the integration of multiplexing, routing, signaling and NoC topologies. TACIT is the only security algorithm that can have ‘n’ bits block size and ‘n’ bits key value. All other existing algorithms such are limited to 128 bits block size and 256 bits of key size. TACIT algorithm is not integrated yet with any network, as a hardware chip. Mesh topology is the best topology for the scalable network because it has
the maximum routing in comparison to other existing topologies and the integration of the topology with 2D and 3D network can enhance the performance of the network. In the multistage network the congestion can be controlled using programmable switches such as programmable three stage network, programmable four stage network programmable five stage network. As an example, in India, Bharat Sanchar Nigam Limited (BSNL) exchanges are following three stage digital network structures which are not programmable. Programmable structures means entire exchange environment is configured using FPGA or ASIC. For a good system the call handling capacity should be more. The operations relating to call handling are handled by concurrent operations using CPLD and complicated and sequential operations like services handling are handled by Microcontroller/ Microprocessor Systems (MPMC). In traditional Telephone switching systems, it is not possible to increase the extension or junction lines because of limitation of processor or controlling system. Designing the system with higher processors is then not cost effective and is complicated too. Solution for this problem is to implement the controlling system for eight lines in a FPGA and make provision to co-control or cascade to the other FPGA of another eight lines so that it can have as many as possible lines. It is also possible because available FPGAs are not much costly but the programmable switching system is a challenge. Programmable multistage networks like four and five stage will enhance the switching capacity of the network and reduce the blocking probability. By the literature survey, it is clear that multistage network concept of four stage is also utilized in optical communication. Therefore, there is
an ubiquitous requirement of development, study and reconfiguration of IP based multistage telecommunication system

CHAPTER SUMMARY

The chapter explains the literature carried out the findings of various research papers support to carry out the research work on multistage crossbar NoC used for telecommunication switching and reconfigurable programmable NoC. The most important reasons for using NoC architectures are their promise for scalability and programmable network capability. Telecommunication traffic characteristics have been long recognized as playing a major part in multicore systems design. The traffic is passed by multistage network and packets are routed with shortest path under maximum available network. These effects have important consequences for the design of on-chip multimedia systems since self-similar processes have properties which are completely different from traditional short range dependent or Markovian processes that have been traditionally used in system-level analyses. From the literature review, it has been subsequently reported that even the traffic generated by programmable cores consists of multiple program phases. Moreover, the research in this area is behind and lacking due to NoC benchmarks. There are two reasons. First reason is that the applications suitable for NoC platforms are typically very complex. It is common for applications to be partitioned among tens of processes or more in order to allow for evaluations of scheduling, portioning and mapping, etc. Some general purpose Chip Multiprocessors (CMPs) are originally designed for shared memory multiprocessors that can be used to share the communication among processor
and I/Os. Second, with the comparison to traditional research areas like physical reason design, where the design constraints are static, the NoC research requires detailed information about the dynamic behavior of the system, which is very hard to obtain even using detailed simulation or prototyping. As a consequence result, most researchers and designers still rely on synthetic traffic patterns such as uniform random, scheduling, bit-permutation traffic, to stress test a network design. The network design of the telecommunication depends on multistage environment. It can follow the two stage, three stage, four stage and five stage structures. The ability of the network to efficiently disseminate information depends largely on the underlying topology. The simplicity and regularity of mesh structures makes design approaches based on such a modular topologies very attractive and much applicable in telecommunication network, the data routed in it is in packet form. Performance analysis of networks largely depends on various simplifying assumptions on the network or traffic characteristics such as uniform traffic vs. bursty traffic and typically assumes deterministic routing due to the difficulty in handling the more general problem. NoC architecture follow mesh, tree, torus and hierarchical structure, depends on the applications is under design. A flexible FPGA based NoC design that consists of processors and reconfigurable components can be integrated into a single NoC chip. The blocking probability, switching elements, switching capacity of the crossbar multistage telecommunication network can be optimized using reconfigurable NoC. The NoC structure can be synthesized on Xilinx supporting FPGA, used to implement programmable multistage network.