CHAPTER-1
INTRODUCTION

The chapter describes the introduction of digital telephony and programmable telecommunication networks. The need of work and motivation of multistage telecommunication networks is discussed. It also includes the problem statement, objectives, supporting parameters for software, hardware and theoretical background. The methodology and design flow is also discussed in the chapter.

1.1 INTRODUCTION TO DIGITAL TELEPHONY

Digital telephony [1, 2] refers to the telephone exchange environment, in which the telephone operations are controlled using digital signals. US organization Bell Laboratories introduced the first digital computer control switching system named as Electronics Switching System (ESS) No. 1 [42, 96]. Modern computers follow the concept of Stored Program Control (SPC) [2], in which, a set of instructions or program is stored in its memory and processor executes the instructions one by one automatically. All the control functions of the exchange are executed through programs stored in the memory is called stored program control. SPC technique in ESS allowed the new features such as call dialing, call waiting, abbreviated dialing [46] and three way calling facility. In
electronic exchange, call processing is handled by the different software, which are used to create and terminate every call by the main system call process. Telecommunication networks are used to route the calls with different stages. As the user dials the number, it is processed by the network. Telecommunication network requires more switching nodes to establish the connections, but achieves significant savings in the number of trunks. A switching network [2, 91] can be made up of single stage or multistage switching [91] blocks which are distributed through intermediate frames. The number of interconnections differs from exchange to exchange.

Telecommunication wired network require routing equipment, bandwidth requirement, set of unique protocols and bandwidth growth rate. For example, the telecom industry has typically increased bandwidth in increments of roughly four (2.5 Gbps to 10 Gbps, now moving to 40 Gbps), while computer networking has done the job in leaps of 10 x (100M, 10G, 100G) [10]. There is the requirement of sophisticated equipment’s such as switches [3], routers [1, 5] and transport systems with advanced circuitry to transport data at these bandwidths. For example, a series of line cards are the heart of a metro router. Under a wide set of protocols, line card [46] receives data packets and examines the packets for size, origin, destination along the network. There is the requirement to complete all functions and computations in nanoseconds.

Telecommunication networks demands high speed switching to deploy and create new and novel services. High speed switching does not depend on the service provider’s operational infrastructure [8] but it depends on the flexibility of
the software architecture. Current telecommunication networks are based on the network structure based on architecture over 30 years in age [42]. The architecture has less computational capabilities and bandwidth is a factor for degree of flexibility. The network switching can be increased using cluster based models where large processors are distributed over the network and to provide distributed services [91]. Dedicated processors used monolithic software [10], which control the response, necessary data and coordinate with the services modules. Traditional communication fabrics [91] have scalability issues in terms of performance and physical circuit design. Networking concept can be brought on chip domain in terms of Network-on-Chip (NoC) paradigm [1] [5], which resolve the concern with a scalable design, at both physical and architectural levels. The NoC system [6] [7] [16] is the combination of different processing blocks which can operate at different clock frequencies and timing requirements. Synchronization is required to communicate among all processing blocks.

The general operation of a switch is to set up and release a connection between two communication entities. Single stage space division network [8] has the limitations that the numbers of crosspoint switches required are prohibitive [91], the no of possible paths are N (N-1) for a square array and N (N-1)/2 for a triangular array [42]. The utility of one crosspoint is that it can be utilized for only one inlet/outlet pair connection. If the connection is failed, there is not any alternative path to communicate with destination subscriber. In a telephone exchange one crosspoint should be utilized to establish more than one connection. It is possible to increase the utilization efficiency of crosspoints, if they are shared
for more than one connection. This work focuses on the chip design and synthesis of four and five stage multistage networks. The networks should be realized in full duplex mode and full available network. The reason to opt the four and five stage networks is to increase the switching capacity of telecommunication network in optimal hardware solution. The design is carried out using Xilinx ISE design suit 14.2 version and functional simulation is done in Modelsim 10.1b student edition software.

1.2 NEED & MOTIVATION

There are three basic elements in the communication network, switches, terminals and transmission media. Electronic switching system (ESS) [1] or Electronics Automatic Exchange (EAX) [2] is used to control the switching functions of a central office. In a single stage space division network, the specific connection between two subscribers was established with the help of a crosspoint switching element [91]. If the switching element is failed, a conversion is not possible between two subscribers. In a multistage space division network, the conversion could be established via any one of the many alternative paths or a crosspoint can be utilized to provide more than one connection. A switching element, once allotted, remains dedicated to a connection for its entire duration because a continuous analog speed signal is passed through the switch in space division switching.

Telephone exchanges are automatic and use electronic switching where all the functions of the network operations are controlled with the help of processors. There are different memories and registers, used to store the information of
source, destination subscriber and data. The information is stored using SPC technique. Call operations and controlling functions in an exchange, largely depends on the line cards associated with these processors. If any of line cards gets failed, no communication remains intact. It is because that the processor is not configured using programmable chips. Although telephone exchanges are digital, they are not yet fully programmable. Programmable structures help in replacement of the chip. It also provides the possibility to reprogram for the specific operation, rather than changing the processors [28]. Thus the need for the programmable network is eminent.

In addition to the non-programmability, telephone exchanges are complex in structure and crossbar switches are larger in size. These factors lead to the traffic congestion in a network [67]. Network switching capacity depends on the number of route available for inlet to outlets. Till today conventional telephone switching is limited to three stage switching. Increasing number of stages in a conventional network is not the feasible solution as it further adds to the hardware complexity along with larger crossbar switches [17, 91]. This limitation can be overcome by the increasing the number of stages such as utilizing four and five stage with programmable network configurations and switching capacity of a network can be enhanced considerably.

In digital transmission, sampled values of the speech are sent as Pulse Amplitude Modulated (PAM) values or Pulse Code Modulated (PCM) binary words. A sampled value should be transmitted from an inlet to outlet in a few microseconds or even less, through a switching element. If one can provide a
dynamic control, where a switching element can be assigned to a number of inlet and outlet pairs, it can be shared by a number of active speech circuits simultaneously in time domain. A switching element can also be made programmable according to the route. It will be greater saving in terms of hardware. Also the integration of multistage switching with time division [46, 91] will improve the efficiency and switching capacity of telephone exchange. A telephone exchange operates 24 hours in a day, 365 days and numbers of years without interruption [5]. This in turn dictates that the exchange should be highly tolerant to control the faults. Early commercial computers were unknown to fault tolerant features [4, 19] and switching engineers had the problem with the development of software and hardware for fault tolerant.

The motivation of digital machines was to reduce manufacturing cost, reduced floor area, low maintenance and simplified expansion. Interoffice transmission was changed to complete digital in mid 1980s and analog switches were replaced to digital. Analog toll [2] and end offices transmission swing to digital conversion cost moved from the associated digital transmission links. The associated trunks with interoffice were already digital. So digital loop carrier system was a cost effective solution in metropolitan applications and digital fiber [14] can be used at the feeder points. Today, all exchanges are based on the SPC, which is an attempt to replace the space division electromechanical switching matrices by semiconductor cross point matrices. Speed, size and cost are three important factors while designing the electronic system. Microprocessor/microcontroller (MPMC) [46]) system can handle sequential
operations with high flexibility and use of Field Programmable Gate Array (FPGA) can handle concurrent operations with high speed in small size area. Thus system performance can be enhanced with the combination of these features. The combination of SPC and its implementation in Hardware Description Language (HDL) environment leads to Programmable Telephone Switching System (PTSS) [3]. PTSS can be designed as a combination of stored program control (SPC) and VLSI technology. As already mentioned, that in telephone switching systems [2, 46], it is not feasible to increase the junction or extension lines [42, 46] because of limitation of processor or controlling system as it will not be cost effective and hardware requirement is more. With the implementation of the controlling system for eight lines in a FPGA and then provides the provision to co-control or cascade to the other FPGA of another eight lines will rectify the above issue.

NoCs support efficient on-chip communication [6, 7] potentially leads to NoC based multiprocessor systems characterized by high structural complexity and functional diversity. Multiprocessor System On-Chip (MPSoCs) [8] consists of complex integrated components, which communicates with each other at very high speed rates. A single shared bus or hierarchies of buses are not feasible for intercommunication. Intercommunication requirements of MPSoCs is made up of about hundred cores having poor scalability with their shared bandwidth between all the attached cores, system size and the energy efficient requirements of final products. NoCs are a promising solution to the scalability problem of forthcoming MPSoCs [5, 9, 10]. NoC is an approach for designing the telecommunication subsystem between IP cores in a System on Chip (SoC) [10, 13]. The software
and application layer is a very critical aspect on the NoC communication stack [11]. Secured transmission among nodes is possible if it follows the NoC layer protocol [14, 19], mostly physical and network layers. All networked layers follow the pipeline and parallel processing that validate the optimized hardware parameters on chip development.

The network design and routing of the telecommunication system depends on multistage switching architecture followed by two stage, three stage, four stage and five stage structures [91]. A flexible FPGA based NoC design that consists of processors and reconfigurable components can be integrated into a single NoC chip. The blocking probability, switching elements, switching capacity of the crossbar multistage telecommunication network should be optimized for reconfigurable NoC structures. Secured data transmission is an issue, when the data is routed through network. Secured transmission can be guaranteed, if the concept of encryption and decryption can be integrated in the NoC chip. In such a case the data is locked at transmission end and is retrieved at the receiving end. The NoC structure can be synthesized on Xilinx supporting FPGA which is used to implement programmable multistage network [102]. For these reasons, research can be emphasized to increase the switching capacity and to increase the communication lines and reduction in blocking probability in four and five stage multistage networks. The integration of network security algorithm with multistage network chip will enhance the system performance and security [84].
1.3 PROBLEM STATEMENT

On the basis of the above mentioned research gaps there was a stringent requirement to carry out the systematic study on such reconfigurable networks. It formulates and defines the problem statement as “Design, Validation and Field Programmable Gate Array (FPGA) implementation of Multistage Telecommunication Network in Hardware Description Language (HDL) Environment”

Problem statement includes the chip design, modeling, simulation and FPGA synthesis of multistage telecommunication network on chip. VHDL has been chosen as the HDL language.

1.4 OBJECTIVES

The objective of the research work is to design the N-stages network and to optimize the hardware parameters. This work also includes the comparison of the obtained parameters with different stages network parameters. FPGA implementation of N-stages network is carried out to validate the results. VHDL programming is used to implement the hardware of N-stages networks starting from single stage, two stage, three stage, four stage and five stage networks. In particular, following are the key objectives to reduce the blocking probability and to increase the switching capacity.

- To design the network in VHDL environment by optimizing the switching parameters

  *Blocking probability*

  *Increasing the calling / switching capacity*
To reduce the existing hardware

- Virtex-5 FPGA synthesis and experimentation on FPGA platform.
- To validate the programmable switching system results with switching parameters
- Integration of network security with multistage network.

1.5 PARAMETERS SUPPORTING TO CHIP DEVELOPMENT

The parameters relating to chip design, modeling, simulation and FPGA implementation [11, 21] and validation are the followings:

- **Synthesis Options Summary:** Synthesis includes the functional simulation and logic optimization. Register Transfer level (RTL) is the chip view, extracted after the modeling of the chip, contains all the possible inputs and outputs, using those pins the chip is developed.

- **VHDL Compilation:** The compilation depends on the approaches used in the designing of the chip whether it is used the top down approach or bottom up approach. It depends on the simulation software used for the chip development. In the research work, the simulation tool is Xilinx ISE Design Suite 14.2.

- **VHDL Analysis:** The VHDL analysis depends on the simulation environment used to check the functionality of the chip developed.

- **Device utilization summary:** Device utilization report gives the percentage utilization of device hardware for the chip implementation. Device hardware includes, logic gates, buffers, multiplexer, decoders, latches, flip flops etc. Synthesis report shows the complete details of device utilization.
• **Timing report and delay time calculation:** Timing details provides the information of delay, minimum period, minimum input arrival time before clock and maximum output time required after clock, and time required to propagate the input to the output.

### 1.5.1 HARDWARE PARAMETERS

The hardware parameters are realizing in terms of FSM encoding, decoding, combinational and sequential logics development. The brief description of each parameter is discussed sequentially.

• **FSM Encoding Algorithm:** FSM encoding determines the FSM [101] coding technique should be used to configure the design. Possible FSM encoding algorithms are auto, one hot, compact, sequential, and gray. Auto encoding selects the needed optimization algorithms during the synthesis process. In one hot encoding, the numbers of flip flops are based on the number of states. For an example, a 31 sates FSM will have 31 flip flops after synthesis. It is advantageous because only one flip flop is hot or active during one state transition. Therefore, it has low power with each state. Binary encoding takes ‘n’ flip-flops for $2^n$ states. Binary coding will take 5 flip flops to cover 31 states, but the disadvantage is that decoding logic is complex. Compact encoding Minimizes the number of state variables and flip flops and is based on hypercube immersion. Sequential encoding consists of identifying long paths and applying successive radix two codes to the states on these paths. Next state equations are minimized. Gray encoding guarantees that only one state variable switches between two consecutive states.
• **FSM Style:** It specifies whether to map the FSM LUTs or block RAM. By default, FSM style is set to LUT.

• **RAM Extraction:** The parameter is relating to the amount of RAM memory utilized in the chip implementation, it is extracted from device utilization report.

• **RAM Style:** The parameters is relating to the type of RAM memory developed, single port RAM, double port RAM and single clocked RAM, double clocked RAM. It can be Auto, distributed or block RAM. In auto XST uses best implementation for each macro. In distributed RAM, memory is distributed in different sizes. In block RAM, entire memory is implemented in different blocks of same size.

• **ROM Extraction:** This parameter relates to the amount of ROM memory utilized in the chip implementation, it is also extracted from device utilization report.

• **ROM Style:** It is related to the ROM type which is developed. It gives the information that weather generated ROM is based on single clock pulse or double clock pulse. ROM memory also can be auto, distribute or block.

• **Mux Extraction:** This parameter relates to the number of multiplexers used in the chip implementation, it is also extracted from device utilization report.

• **Mux Style:** In the chip integration, RTL internal view the logic can be configured using 2 x 1 mux, 4 x 1mux, 8 x 1 mux and 16 x 1 mux, or depends on the logic inputs required to configure the structure.
• **Decoder Extraction:** Decoder is the essential part of the network structure which is utilized in the address selection of the node in NoC design.

• **Priority Encoder:** Selection logic to assign the priority which accepts $2^n$ inputs and extract the data of ‘n’ bits.

• **Shift Register Extraction:** Used to select the number of shift registers used, it depends on the no of flip-flops used to store the information.

• **Logical Shifter Extraction:** Based on shifting operations like left shift, right shift, rotate left and rotate right operations logical shifter is selected.

• **XOR Collapsing:** how many numbers of XOR gates are required, can be found by synthesis report.

• **Resource Sharing:** it contains the information of number of interconnecting logic used for implementing the chip.

• **Multiplier Style:** Used to identify the number of multipliers used in the chip development.

• **Automatic Register Balancing:** Optimal number of buffer registers used to store the data.

• **DSP blocks:** A DSP block provides optimal solution for DSP operations with maximum functions and minimum logic resource utilization. Each DSP block consists of adders, multipliers, accumulators, subtractors and a summation unit. Each DSP block can support a variety of multipliers vary in size (9 x 9, 18 x 18, 36 x 36), operation modes such as multiplication, complex multiplication, multiply-addition and multiply-accumulation.
1.5.2 FPGA PARAMETERS

The parameters related to the hardware synthesis and logic optimization are called FPGA parameters.

- **I/O Buffers:** Add I/O Buffers is the target option for Xilinx Synthesis Technology (XST) to add or not add Input Buffers (IBUF), Output Buffers (OBUF) or Input Output Buffers (IOBUF) on the top level ports. By default, it is enabled because each design requires I/O buffers on the top level port. In a sub module synthesis, it needs to disable because I/O buffer should be in the top level.

- **Global Maximum Fan-out:** The maximum fan-out of an output measures its load-driving capability. For Virtex 5 FPGA device, max fan-out is default 100000. If the value of max fan-out synthesis is changed, it will be applied globally and affect the whole design.

- **Generic Clock Buffer (BUFG):** In Xilinx design, the programmer uses global clock buffers to take advantage of the low-skew, and high-drive capabilities. Whenever an input signal drives a clock signal, FPGA Compiler automatically inserts a generic global clock buffer (BUFG). The Xilinx implementation software automatically selects the clock buffers, which are appropriate for specified design constraints.

- **Register Duplication:** This parameter moves registers through combinatorial logic to evenly distribute the path’s delay between registers. It is also called as flip-flop retiming. In the process, both forward and backward retiming are
possible but XST does not perform flip flop retiming. It specifies whether or not the designer want to replicate the register to help control fanout.

- **Slice Packing**: XST currently has a "Slice Packing" switch, help in grouping LUTs into slices during optimization. It does not provide only more accurate timing information for optimization, but it is also passed to implementation for maintain more consistency during mapping.

- **Optimized Instantiated Primitives**: It is the default mode, which allows XST to perform efficient optimization across module boundaries. If the designer needed, it is possible to keep Hierarchy in synthesis.

- **Use Clock Enable**: XST optimizes the logic such that the clock enable signal and reset condition are combined and fed to the reset input of the counter. The property specifies whether or not clock enable pins are utilized by XST. When clock enable is set to auto mode, XST uses dedicated clock enable pins on inferred registers if they provide a benefit to the overall quality of the design. When it is set to yes, clock enable pins are used in flip-flops. When set to No, there is no use of clock enable pins, and the corresponding functionality is implemented in standard logic.

- **Use Synchronous Set**: Synchronous set is synchronized with clock and specifies whether or not synchronous set pins are utilized by XST. When the pin is set to auto mode, XST uses dedicated synchronous set pins on inferred registers if they provide a benefit to the overall quality of the design. When it is set to Yes, synchronous set pins are used in flip-flops. When set to No, there
is no utilization of synchronous set pin, and the corresponding functionality is implemented in standard logic.

- **Use Synchronous Reset**: Synchronous reset is synchronized with clock and specifies whether or not synchronous set pins are utilized by XST. If reset is done all the contents of flip flops are zero.

- **Pack IO Registers into IOBs**: It controls the IOB flip flop merging capabilities. This option forces all flip-flops connected to pads into the IOB, whatever possible. In auto mode, this option uses the timing offsets and periods specifications to determine if IOB flip-flop merging should be done. In no condition, it prevents IOB flip-flop merging from occurring.

- **Equivalent register Removal**: For the optimization of flip-flops the property is utilized. Flip-flop optimization includes the removal of flip-flops and equivalent flip-flops with constant inputs.

### 1.5.3 GENERAL PARAMETERS

The general parameters are related to RTL, module hierarchy, netlist generation, memory and slice utilization and are given below:

- **Optimization Goal**: The optimization parameters for the chip are speed, cost, delay and power consumption.

- **Optimization Effort**: Speed Optimizes the design for speed by reducing the levels of logic and area optimizes the space for area by reducing the total amount of logic used for design implementation.

- **RTL Output**: Chip synthesis optimizes the design using minimization and algebraic factoring algorithms. Additional optimizations are tuned to the
selected device architecture and higher multiple optimization algorithms are used to get the best result for the target architecture. If the designer need to optimize the inputs and outputs of the chip, it is possible with the help of RTL.

- **Keep Hierarchy:** This property specifies whether the corresponding design units merged with the rest of the design. It can be No, Yes and Soft. Soft is used when the designers want to maintain the hierarchy through synthesis.

- **Netlist Hierarchy:** Netlist hierarchy controls the form in which the final netlist is generated. It allows the designer to write the hierarchical netlist even if the optimization was done on a fully or partially flattened design.

- **Global Optimization:** Global optimization specifies the global timing optimization goal. There are some properties for global optimization which are All Clock Nets, inpad to outpad, offset in before, offset out after and maximum delay. All Clock Nets optimizes the period of the entire design. inpad to outpad optimizes the maximum delay from input pad to output pad throughout an entire design. Offset in before optimizes the maximum delay from input pad to clock, either for an entire design or for a specific clock. Offset out after optimizes the maximum delay from clock to output pad, either for a specific clock or for an entire design. Global optimization will be also set to maximum delay constraints for paths from staring input to output.

- **Slice Utilization Ratio:** It specifies the area in percentage that XST will not exceed during timing optimization. XST will make timing optimization, if the
area constraint cannot be satisfied. Default, the designer keeps this ratio 100%.

- **BRAM Utilization Ratio:** It specifies the number of BRAM blocks in percentage XST will not exceed during timing optimization. Default, the designer keeps this ratio 100%.

- **Auto BRAM Packing:** It specifies whether or not XST will try to pack two small single-port BRAMs into a single BRAM primitive, to form dual-port BRAM. If BRAMs are at the same hierarchical level in the design, only then can be packed together.

- **Slice Utilization Ratio Delta:** This constraint defines the percentage of slices XST can use to implement the design or a block of designer’s need.

### 1.5.4 PERFORMANCE PARAMETERS

Performance parameters for a lossy system are the grade of service (GOS) and the blocking probability (P_B) and switching capacity [4, 91]. The parameters depend on the traffic congestion, routing delay and network cluster or population size.

- **Grade of Service (GoS):** In lossy system, the network carries less traffic than the actual traffic offered to the network by the subscribers. The overall traffic is rejected and is an index of the quality of service offered by the network. This is known as grade of service (GoS) [46] and it is the ratio of lost traffic to offered traffic.

\[
\text{GoS} = \frac{\text{Lost Traffic}}{\text{Offered Traffic}}
\]
GOS = \frac{A - A_0}{A} \quad \text{Equ. 1.1}

Where

\( A_0 \) = Traffic carried by the network.
\( A \) = Offered traffic to the network

- **Blocking Probability \((P_B)\):** Blocking probability is the probability that all the servers in a system are busy. When all the servers are busy, the network will not carry any further traffic and arriving subscriber traffic is blocked. The probability that all the servers are busy may be presented by calls lost.

\[ \text{Blocking Probability \((P_B)\)} = \text{Congestion probability} \]

Blocking probability is calculated using Poisson process. The governing equation of a Poisson Process is [11]

\[ P_k(t) = \frac{(\lambda t)^k e^{-\lambda t}}{k!} \quad \text{Equ. 1.2} \]

Where \( \lambda \) = Calls per second, the value of ‘t’ is taken from the device utilization report as the value of minimum time.

- **Switching Capacity:** The total capacity of public switching exchanges corresponds to the maximum number of fixed telephone lines that can be connected. Therefore, this number includes fixed telephone lines already connected and fixed lines available for future connection, including those used for the technical operation of the exchange. The measure should be the actual capacity of the system, rather than the theoretical potential when the system is upgraded or if compression technology is employed. Switching capacity is
the capacity of the multistage network when it is full connected and full available network.

1.6 METHODOLOGY & DESIGN FLOW

The methodology comprises the different steps which are carried out for the design and development of chip. The model is shown in figure 1.1.

![Diagram](image)

Fig. 1.1 Steps in methodology
• **Design Specification:** In design specifications the designer decides to develop the chip either in top down or bottom up approach. In bottom up approach the circuit is designed using micro module to form a design and top down approach a design is distributed in sub modules. In the multistage networks bottom up approach is utilized to implement the design.

• **Network Configuration:** The designer has to choose the cluster size of the design. In the case of multistage network, the network configuration needs to be decided. For example, for single stage , two stage, three stage, four stage and five stage networks the network configuration is 2 x 2, 4 x 4, 8 x 8, 16 x 16 or more with respect to inlets and outlets respectively.

• **HDL Modeling:** The designer has to understand the feasibility to design with the supporting languages such as VHDL, Verilog HDL, and System C etc. The designer also decides the modeling of chip and design constructs in data flow, behavioral and structural model.

• **Functional Simulation:** The designed modules are checked according to their functionality and test cases. The functional simulation depends on the test benches developed by the designer, clock frequency and reset circuitry.

• **Pre Synthesis:** Pre synthesis includes the RTL simulation, device synthesis report contains the summary of hardware parameters with combinational and sequential circuit. If the hardware utilization is greater than the 100 % for the configured device, the designer has to redesign and check for the optimized device and timing parameters.
• **Experimentation and FPGA Synthesis:** The experimental setup is arranged to check the functionality of chip with its compatibility and interfacing to FPGA board. The maximum support frequency of FPGA board is analyzed to check the data transfer rate. In the experimental setup inputs can be through switches, and output can be analyzed with the help of LEDs. There is inbuilt ADC and DAC in Virtex 5 FPGA to check the real time functionality.

• **Parameters Analysis:** The FPGA source and target parameters are analyzed with the help of optimized FPGA results. Static timing analysis and device utilization is also analyzed with minim speed grade and memory utilization.

• **Testing:** The synthesized results are tested for the different test cases and combination with the help of LUTs. In the multistage network the inlets and outlets functionality is checked for maximum combination, inert and interexchange communication. The developed chip is also tested for analog input given to FPGA and processed output signals on DSO. The signal characteristics are also tested with the FPGA device compatibility and display unit.

• **Verification:** The Design Under Test (DUT) is verified with timing parameters and test cases. Standard VHDL has all the features necessary to code randomization of stimulus and functional coverage, both are very important while verifying larger, system-level designs. Verification is used to describe testing of a group of logic using a test bench, implemented for every verification level. The most common verification levels are SoC verification level, sub SoC verification level with a group of IP blocks, IP block
verification level building test benches around IP blocks. IP blocks verification allows greater control to stress internal blocks more heavily than a SoC test bench can provide.

1.6.1 VIRTEX- 5 FPGA DESIGN FLOW

The Virtex 5 family provides the most recent and powerful features within Xilinx FPGA families. There are existing five distinct sub-families of Virtex 5 FPGA. Each platform contains a different ratio of features to address the needs of a wide variety of advanced logic designs. Moreover, in addition to the most advanced features, high-performance logic fabric, Virtex 5 FPGAs contain many hard-IP system level blocks, including powerful second generation 25 x 18 DSP slices, 36-Kbit block RAM/FIFOs, and enhanced clock management tiles with integrated Digital Clock Manager (DCM) and Phase Locked Loop (PLL) clock generators with advanced configuration options. It has additional platform dependant features include tri mode Ethernet Media Access Controllers (EMACs), power optimized high speed serial transceiver blocks for enhanced serial connectivity, and high-performance Power PC 440 microprocessor embedded hard core blocks. The research is based on the FPGA flow shown in figure 1.2.

The first step involves understanding of the design requirements, initial design entry, problem decomposition, and functional specifications where correctness by comparing outputs of the VHDL model and the behavioral model are checked. The multistage network is designed with the help of VHDL programming language. The designed may be based on FSM encoding, state
diagram analysis. Synthesis involves the conversion of an HDL description to a netlist which is basically a gate level description of the design.

In the FPGA synthesis, different optimization constraints are applied to the design. In implementation of the chip, the generated netlist is mapped onto Virtex 5 FPGA device's internal structure using technology libraries. Logic optimization process optimizes Boolean expressions into a standard form to optimize area or speed. Technology mapping minimizes blocks to minimum area. The main phase of the implementation stage is place and route, which allocates FPGA resources. The general FPGA resources may such as logic cells, hard core
blocks, memory, and connection wires. Thereafter, configuration data are written to a special file by a program called bit stream. For timing analysis, there is a special software checks whether the implemented design satisfies timing constraints specified by the designer. In static timing analysis, the actual delay models are used to estimate the real delay on the chip after routing. Routing is helpful to provide connections between cells to minimize area. After the FPGA synthesis the chip is ready to send to foundries for fabrication unit.

1.7 OUTLINE OF CHAPTERS

- Chapter-1 presents the introduction to digital telephony, need & motivation, problem statement, objectives, research model and research methodology.
- Chapter-2 presents the literature review and contributions by the different researchers on multistage network and network security.
- Chapter-3 presents the multistage networks and routing scheme in multistage networks (single stage switching to five stage switching)
- Chapter-4 presents the 3D NoC, Network security and key management policy, used for secured networks.
- Chapter-5 presents the experimental set up and synthesis environment with different testes cases and analysis. The chapter also includes the display of the experimented data.
- Chapter-6 presents the results and discussion. Results include Xilinx 14.2 ISE chip design synthesis report, functional simulation on Modelsim 10.1 b and FPGA synthesis. FPGA synthesis includes device utilization summary, timing parameters. A comparison of FPGA parameters with single stage, two stage,
three stage, four stage and five stage switching network is also included with the chapter. The chapter also includes the statistical simulated data and analysis with optimized hardware and experimental synthesis work on Virtex - 5 FPGA.

- Chapter-7 presents the conclusion and future scope.

CHAPTER SUMMARY

A telecommunications network is a collection of links, terminal nodes, and any intermediate nodes, which are connected so as to enable telecommunication between the terminals. The nodes are connected together using transmission links. The nodes use circuit switching, packet switching or message switching to transmit the signals through the correct links and nodes to reach the correct destination terminal. Individual terminal in the network usually has a separate address so messages or connections can be routed to the correct recipients. Messages are generated by a sending terminal, routed through the network of links and nodes until they arrive at the destination terminal. In telecommunication networks, the message is routed in multistage switching because in single stage switching there is only one dedicated path to establish the connections between source and destination subscribers. In multistage switching, there are alternative ways, in case of failure of dedicated link. All telecommunication networks are made up of five basic components that are present in each network environment regardless of type or use. These basic components include terminals, telecommunication processors, telecommunication channels, computers, and telecommunication control software. The SPC
technique is used to store the data, with the help of processors. The data transfer from one node to another node can be secured if the concept of programmable chips can be integrated with network security algorithms. The switching structures can reduce the hardware used to control the switching operations, with the integration of transmission, routing, signaling and security in programmable chips and make a supervision of control and co control. In the chapter, it has been summarized the need and motivation of programming telecommunication networks with the integration of secured transmission. The general parameters, hardware parameters, theoretical parameters, source and target parameters are also discussed, with the synthesis process on Virtex-5 FPGA.