FAULT DIAGNOSTIC TECHNIQUES FOR VLSI

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ABSTRACT

With the advancement of Very Large Scale Integration technologies there is an increase in speed and density of the integrated circuits. This in turn increases the cost and complexity of tests that are to be performed on digital integrated circuits and systems. Generally, fault diagnosis helps in reducing the area of chip where fault detection is to be performed. Fault diagnosis is basically a process in which tests are applied to the chip that has failed and then analysis of the test's results is done to detect the fault. In diagnosis, a diagnostic test set is very useful. The user applies test vectors to the circuit under test / diagnosis and the output responses are matched with the actual responses. This comparison results in either a match or a mismatch. A match shows that the circuit is working in the desired way but a mismatch concludes a fault in the circuit.

The problem identified in the system is that if there is a requirement of fault diagnosis in a typical system with stuck at faults then algorithm must be there to detect that. Moreover, where speed and time constraints are at priority, then the existing system may prove to be slow since it has single processor. The identified problem has been resolved by using the developed algorithm on the system.

The main focus is to develop a system with parallel processors and detect different faults in it with the help of algorithms. So these have been developed with new technique that would detect the fault and use of parallel processors would improve the speed. The aspect of miniaturization has the requirement to devise a system where speed and time constraints are at priority. In this respect, a system with parallel processors has been developed which consists of four terminals, buffers named FIFO (First in First Out), two processors and multiplexers. Two processors have been used for parallel processing of the data. The data have been stored in FIFO at each

input port. The system with parallel processors has been implemented in VHDL (Very high speed integrated circuits Hardware Description Language) and the existing single processor system has also been implemented in VHDL. The comparisons made in terms of CPU (Central Processing Unit) utilization and memory usage prove the developed system to be beneficial. Moreover, stuck at 0/1 fault has been effectively detected in the system which has been implemented in VHDL as reported in this work.

With the help of developed algorithms the stuck at faults have been detected in a system and with the help of backtrack algorithm it has been traced and the table validates it. Algorithms have also been developed to detect other possible faults in the system such as dropped data fault, multiple copies in space fault and the corrupt data fault.