CHAPTER 3

NINE-LEVEL DIODE-CLAMPED PWM INVERTER WITH FRONT END RECTIFIER FED ADJUSTABLE SPEED DRIVE

A nine-level diode-clamped inverter is proposed for a medium voltage adjustable speed drive with a three-phase diode rectifier used as the front-end rectifier. Three-level neutral-point-clamped or diode clamped inverter was invented in1979. It has been applied to steel mill drives, unified power flow controllers, the Japanese bullet train (the so-called "Shinkansen") and so on. Recently, consideration has been paid to multilevel inverters proposed for high-power and medium-voltage applications. Using IGBT some nine level diode clamped PWM inverter is to reduce bulky transformers from medium-voltage speed drives.

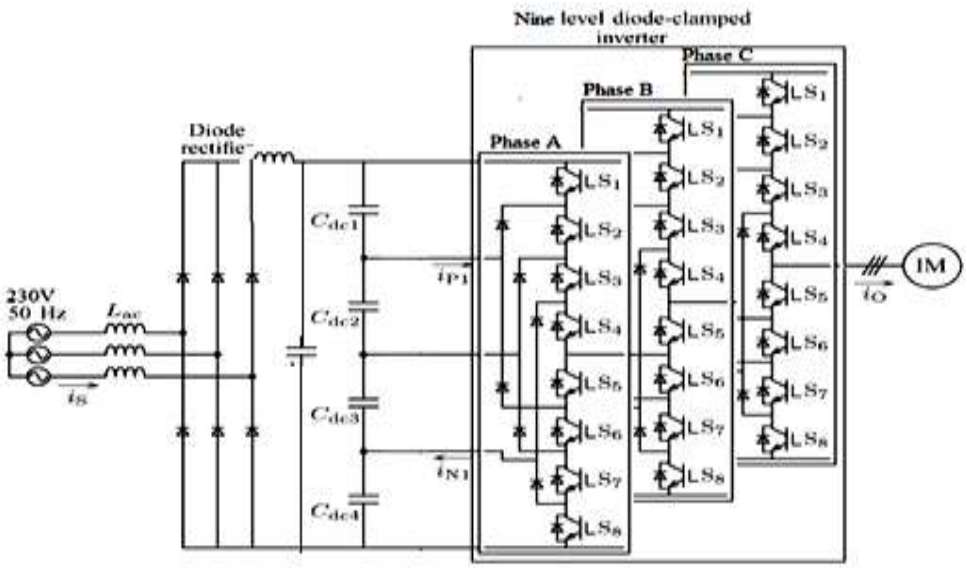

Figure 3.1 Multilevel inverter with front end rectifier

The nine-level diode clamped DC link inverter with front end rectifier is shown in Figure 3.1.DC link inverter is preferred for ASD application to

produce desired voltage and frequencies from a constant AC input voltage. The circuit operation of six-pulse diode rectifier and MLI follows.

3.1 Six pulse diode rectifier

The rectifier PF was improved by reducing the input current THD. A three-phase diode bridge rectifier is explained with relevant voltage waveforms and their spectra derived in this section. Likewise, logic functions that define the condition of the diode in the three-phase diode bridge termed diode state functions are characterized.

In Figure 3.2, a three-phase diode bridge rectifier was presented. It consists of a three-phase diode bridge, involving diodes D1 to D6. AC input voltage converted into DC by each diode conducts for 120°. When the diode gets forward biased start to conduct at the cross over point and harmonics introduced in the input AC supply. In the investigation, it is expected that the impedances of the supply lines are sufficiently low to be ignored and that the load current I_{OUT} is constant in time.

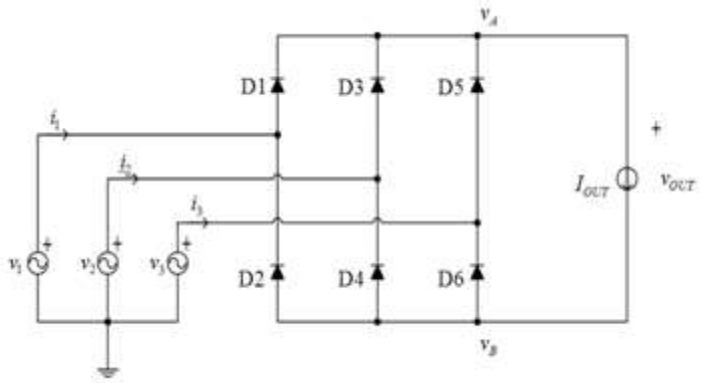

Figure 3.2 Three phase diode rectifier

First, let us assume that the rectifier is supplied by a balanced undistorted three-phase voltage system, specified by the phase voltages v_1,v_2,v_3 and which

are expressed as

$$v_1 = \mathrm{V_m}\cos(\omega_0 \mathrm{t}) \quad (3.1)$$

$$v_2 = V_m cos(\omega_o - \frac{2\pi}{3}) \quad (3.2)$$

and

$$v_3 = V_m cos(\omega_o - \frac{4\pi}{3}) \quad (3.3)$$

The amplitude of the phase voltage V_m is written as

$$V_m = V_{PRMS}\sqrt{2} \quad (3.4)$$

Where,

V_{PRMS} is the root-mean-square (RMS) value of the phase voltage.

It has three legs. Each leg has two series connected diodes. Six diodes are divided into two groups. Upper groups, consisting of diodes, D1, D3, D5, is known as a positive group. It provides three pulses positive output at the point v_a. lower group, consisting of diodes D2, D4, D6, is known as the negative group. It provides three pulses negative output at the point v_b.

The input voltages waveforms are exhibited in Figure 3.3.The phase voltages determined by (3.1), (3.2), and (3.3), two of the phases are connected to the load while one phase is unconnected in each point in time. An input current equal to zero in the time interval when the phase voltage is neither minimum nor maximum. The current injection methods are used to reduce gaps in phase currents. The portrayed operation of the diodes in the diode bridge brings about the maximum of the phase voltage equals to positive output terminal voltage, and it is expressed as

$$v_A = \max(v_1, v_2, v_3) \quad (3.5)$$

The minimum of the phase voltage is equals to negative output terminal voltage, and it is written as

$$v_B = \min(v_1, v_2, v_3) \tag{3.6}$$

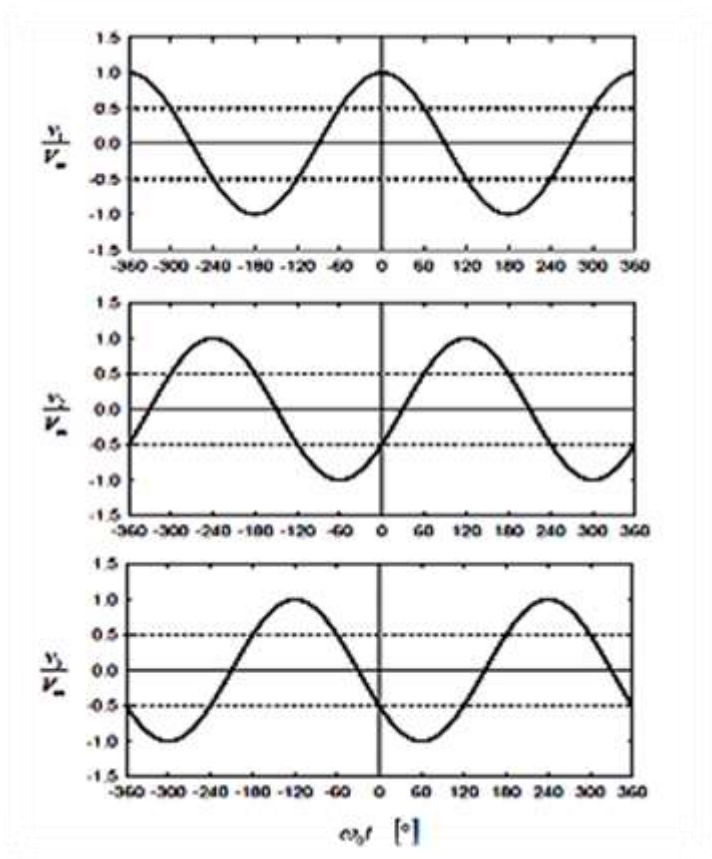

Figure 3.3 Three phase input voltage

The wave forms of output terminal voltages expressed by (3.5) and (3.6) are presented in Figure. 3.4. These waveforms are intermittent, with the period equal to 1/3 of the line period; thus their spectral components are located at three times of the line frequency. The Fourier series expansion of the positive output terminal prompts to

$$v_A = \frac{3\sqrt{3}}{\pi} V_m \left[\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{(-1)^{n+1}}{9n^2-1} cos(3n\omega_0 t)\right] \quad (3.7)$$

While the Fourier series expansion of the voltage of the negative input terminal results in

$$v_B = \frac{3\sqrt{3}}{\pi} V_m \left[-\frac{1}{2} + \sum_{n=1}^{+\infty} \frac{1}{9n^2-1} \cos(3n\omega_0 t)\right] \quad (3.8)$$

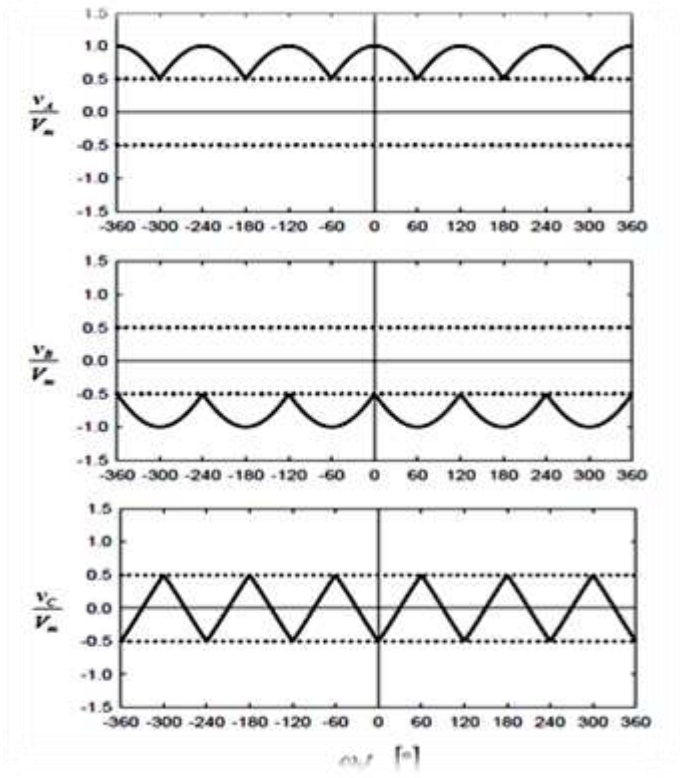

Figure 3.4 Output voltages at terminal V_A, V_B, and V_C

Fourier series expansions are used for various current injection strategies. At the multiples of tripled line frequency, spectral components are present, i.e., at triples of the line frequency. The spectral components of v_A and

v_B at odd triples of the line frequency at $3(2k-1)\ \omega_0$, where $k \in N$, are the same, having the same phases and amplitudes. On the other hand, the corresponding spectral components at even triples of the line frequency, at $6k\omega_0$, have the same amplitudes but inverse phases.

The output voltage of the diode bridge is written as

$$v_{OUT} = v_A - v_B \tag{3.9}$$

and it is displayed in Figure. 3.5. The Fourier series expansion of the output voltage given by

$$v_{OUT} = \frac{3\sqrt{3}}{\pi} V_m \left[1 + \sum_{k=1}^{+\infty} \frac{1}{36k^2-1} cos(6k\omega_0 t)\right] \tag{3.10}$$

Since spectra of v_A and v_B have the same spectral components at odd triples of the line frequency, these spectral components nullify in the spectrum of the output voltage. Accordingly, the spectrum of the output voltage contains spectral components only in 6^{th} multiples of the line frequency. The output voltage DC component equals

$$v_{OUT} = \frac{3\sqrt{3}}{\pi} V_m \approx 1.65 V_m \approx 2.34 V_{PRMS} \tag{3.11}$$

While the AC component of the output voltage is expressed by the Fourier series as

$$v_{OUT} = \frac{3\sqrt{3}}{\pi} V_m \sum_{k=1}^{+\infty} \frac{2}{36k^2-1} cos(6k\omega_0 t) \tag{3.12}$$

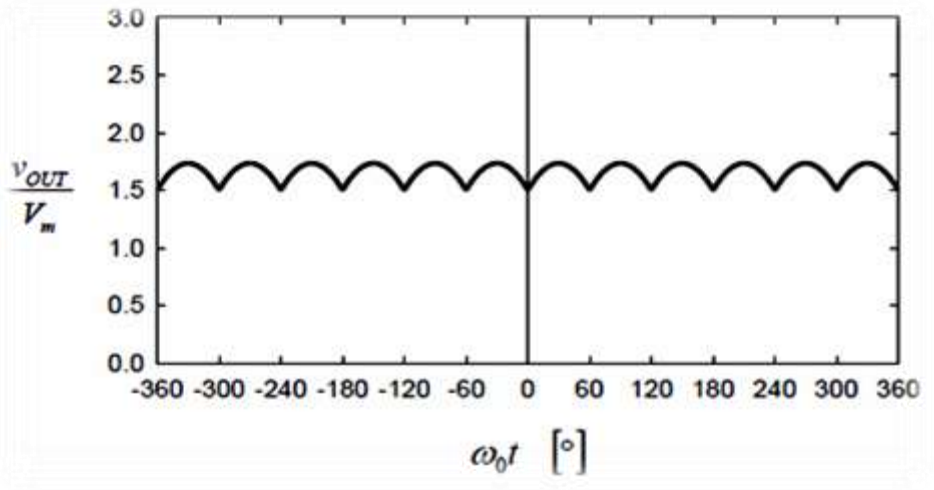

Figure 3.5. Output voltage of the rectifier

In the waveform analysis, the waveform of "the remaining" voltage, v_C, i.e., during the time intervals when they are neither minimal nor maximal, the waveform obtained from segments of the phase voltages. In Figure. 3.2, a node in the circuit where that voltage could be measured does not become available, in contrast to the waveforms of v_A and v_B that can be observed at the diode bridge output terminals. However, by using the fact that the sum of the instantaneous values of the phase voltages equals zero, the spectrum of v_C and waveform can be computed easily. It is described as

$$v_1 + v_2 + v_3 = 0 \tag{3.13}$$

In each point in time, one of the phase voltages equals v_A, another one equals v_B, while the remaining one equals v_C. Thus, the output terminal voltages and "the remaining voltage" add up to zero. This gives the following expression for "the remaining voltage":

$$v_C = -v_A - v_B \tag{3.14}$$

by using spectra of v_A and v_B, the spectrum is computed given by (3.7) and (3.8), resulting in

$$v_C = -\frac{3\sqrt{3}}{\pi} V_m \sum_{k=1}^{+\infty} \frac{2}{(6k-3)^2-1} cos((6k-3)\omega_0 t) \quad (3.15)$$

At odd triples of the line frequency, spectral components are located. Spectral components of v_A and v_B at even triples of the line frequency cancel out.

Another voltage of interest is the average of the output terminal voltages, written as

$$v_{AV} = \frac{1}{2}(v_A + v_B) = -\frac{1}{2} v_C \quad (3.16)$$

Using the spectrum of v_C, given by (3.15), the spectrum of v_{AV} is obtained as

$$v_{AV} = -\frac{3\sqrt{3}}{\pi} V_m \sum_{k=1}^{+\infty} \frac{1}{(6k-3)^2-1} cos((6k-3)\omega_0 t) \quad (3.17)$$

The spectral components of v_{AV} are located at odd triples of the line frequency as same as in the spectrum of v_C. After the waveforms of the rectifier, voltages are defined and their spectra obtained, waveforms of the rectifier currents are studied. Primly, let us define the diode state functions d_k for $k \in \{1,2,3,4,5,6\}$such that if d_k=0 the diode is blocked and d_k =1 the diode conducts. During the two line periods, the diode state functions of waveforms are displayed in Figure.3.6and the state functions of the diode are listed in Table 3.1. From the Table 3.1data, it can be summarized that the rectifier of Figure.3.2.The analysis significantly simplifies because it was analyzed as a periodically switched linear circuit since the states of the diodes are written as functions of the time variable. The discontinuous conduction mode of the diode bridge is studied, though with significant mathematical difficulties, since the circuit can't be dealt with as a periodically switched linear circuit. After the diode state functions are defined, currents of the diodes can be written as

$$i_{Dk} = d_k(\omega_0 t) I_{OUT} \quad (3.18)$$

For $k \in \{1,2,3,4,5,6\}$. The current waveforms of all diodes have the same average value

$$I_D = \frac{1}{3} I_{OUT} \quad (3.19)$$

Table 3.1 Diode state function

Segment	Conducting diodes
$0<\omega_0 t<60^0$	D1 and D6
$60^0<\omega_0 t<120^0$	D3 and D6
$120^0<\omega_0 t<180^0$	D2 and D3
$180^0<\omega_0 t<240^0$	D2 and D5
$240^0<\omega_0 t<300^0$	D4 and D5
$300^0<\omega_0 t<360^0$	D1 and D4

Which is of interest for sizing the diodes. The maximum of the reverse voltage that the diodes are exposed to is equal to the maximum of the output voltage and equal to the line voltage amplitude,

$$V_{Dmax} = V_m\sqrt{3} = V_{PRMS}\sqrt{6} \quad (3.20)$$

Using the diode state functions, the rectifier input currents i_p, where

$p \in \{1, 2, 3\}$ can be expressed as

$$i_p = I_{OUT}(d_{2p-1}(\omega_0 t) - d_{2p}(\omega_0 t) \tag{3.21}$$

Waveforms of the input currents are presented in Figure 3.7. The input currents have the same RMS value, equal to

$$I_{RMS} = \frac{\sqrt{6}}{3} I_{OUT} \tag{3.22}$$

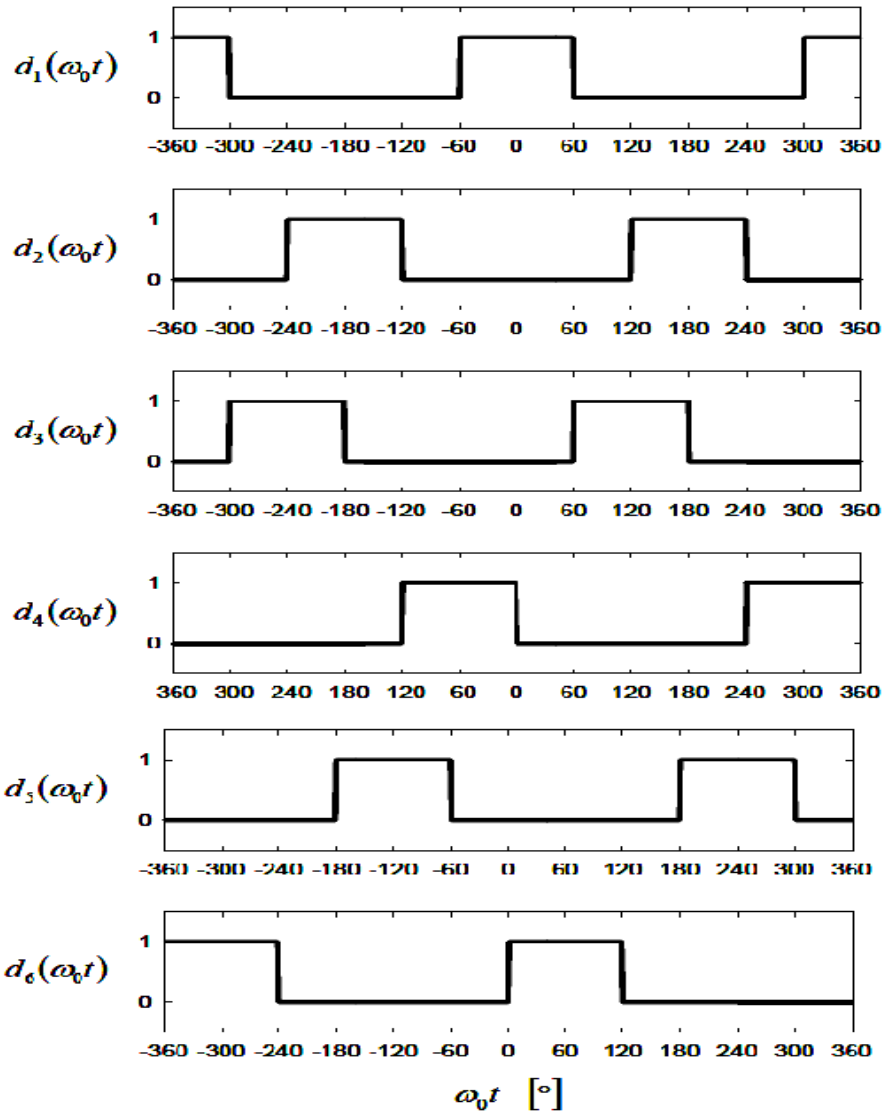

Figure 3.6 Diode conduction state function

Output power of the rectifier is expressed as

$$P_{OUT} = V_{OUT}I_{OUT} = \frac{3\sqrt{3}}{\pi}V_m I_{OUT} = P_{IN} \quad (3.23)$$

The losses in the rectifier diodes are neglected in this analysis, and there are no other elements in the circuit of Figure. 2.1 so the input power P_{IN}, is same as output power. At the rectifier input, the apparent power expressed as

$$S_{IN} = 3V_{PRMS}I_{RMS} = \sqrt{3}V_m I_{OUT} \quad (3.24)$$

From the rectifier, apparent power and rectifier input power are given by the equation (3.24) and (3.23) respectively. At the rectifier input, the power factor is acquired as

$$PF = \frac{P_{IN}}{S_{IN}} = \frac{3}{\pi} = 0.9549 \quad (3.25)$$

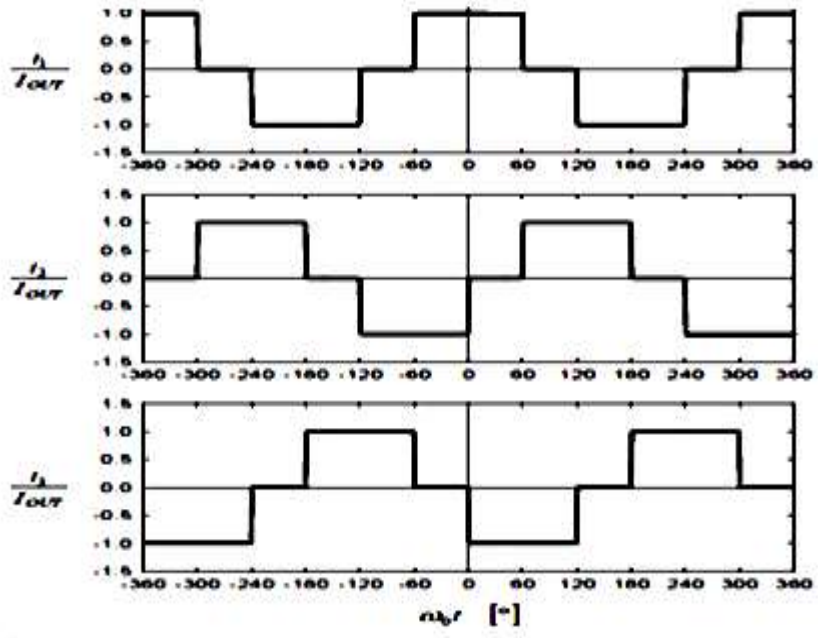

Figure 3.7 Input current waveforms

The above value of power factor is reasonably good and fulfills almost all of the power factor standards. It is significantly better than the power factor value of the rectifier with the capacitive filter connected at the output, which forces the rectifier to operate in the discontinuous conduction mode. The result is also good in comparison to single-phase rectifiers. Subsequently, the power factor value as given in equation 3.25 is not ideal. The parameter of the rectifier of Figure.3.2 on which attention is given for total harmonic distortion (THD) of the input currents. To compute the THD values of the input currents, the RMS value of the input current fundamental harmonic is determined as

$$\mathrm{I_{1RMS}} = \frac{\sqrt{6}}{\pi}\mathrm{I_{OUT}} \tag{3.26}$$

The fundamental harmonic input current displaced to the corresponding phase voltages for being

$$\varphi = 0 \tag{3.27}$$

Which results in the Displacement Power Factor (DPF)

$$\mathrm{DPF}=\cos\varphi = 1 \tag{3.28}$$

The THD of the input currents is determined to apply

$$THD = \frac{\sqrt{{I_{RMS}}^2 - {I_1}^2{}_{RMS}}}{I_{1RMS}} \tag{3.29}$$

Resulting in

$$THD = \frac{1}{3}\sqrt{\pi^2 - 9} = 31.08\% \tag{3.30}$$

This THD value is considered high. The main aim of this work is to analyze efficient methods to diminish the THD value of the input currents in three-phase diode bridge rectifier.

Some standards limit amplitudes of particular input currents harmonic components. So, the input currents spectrum can be expressed by Fourier series expansions of the form

$$i(t) = I_{DC} + \sum_{n=1}^{+\infty}(I_{C,n}\cos(n\omega_0 t) + I_{S,n}\sin(n\omega_0 t) \quad (3.31)$$

$$= I_{DC} + \sum_{n=1}^{+\infty} I_n \cos n\omega_0 t - \varphi_n$$

Where,

$$I_{DC} = \frac{1}{2\pi}\int_{-\pi}^{\pi} i(t)d(\omega_0 t) \quad (3.32)$$

$$I_{C,n} = \frac{1}{\pi}\int_{-\pi}^{\pi} i(t)\cos(n\omega_0 t)\, d(\omega_0 t) \quad (3.33)$$

$$I_{S,n} = \frac{1}{\pi}\int_{-\pi}^{\pi} i(t)\sin(n\omega_0 t)\, d(\omega_0 t) \quad (3.34)$$

$$I_n = \sqrt{I_{C,n}^2 - I_{S,n}^2} \quad (3.35)$$

and

$$\tan\varphi_n = \frac{I_{S,n}}{I_{C,n}} \quad (3.36)$$

In the case of the first phase of input current, expressed by equation 3.21.

For p =1, the harmonic components are

$$I_{1,DC} = 0 \quad (3.37)$$

$$I_{1,C,n} = \frac{2}{\pi n}\left(\sin\frac{2\pi n}{3} + \sin\frac{\pi n}{3}\right)I_{OUT} \quad (3.38)$$

$$I_{1,S,n} = 0 \quad (3.39)$$

Thus

$$I_{1,n} = \frac{2}{\pi n}\left|\sin\frac{2\pi n}{3} + \sin\frac{\pi n}{3}\right| I_{OUT} \quad (3.40)$$

and

$$\varphi_n = \frac{\pi}{2}\left(1 - sgn\left(\sin\frac{2\pi n}{3} + \sin\frac{\pi n}{3}\right)\right) \quad (3.41)$$

$$i_1(\omega_0 t) = i_2\left(\omega_0 t - \frac{2\pi}{3}\right) = i_3\left(\omega_0 t - \frac{2\pi}{3}\right) \quad (3.42)$$

The waveforms of the input currents of the remaining two phases of the rectifier are displaced in phase by 2π/3 in comparison to one another, according to equation 3.42.Thus, by using the time-displacement property in Fourier series expansions, all of the input currents share the same amplitude spectrum but have different phase spectra.

From the waveforms, it is summarized that the voltage system is balanced, but the voltages are distorted slightly in the form of two deviations: notches and flattened sinusoid tops. By single-phase, rectifiers with capacitive filtering caused flattened tops of the waveforms, and this type of distortion is not caused by the analyzed rectifier. However, by commutations in the diode bridge and the nonzero line impedance, notches are caused. This commutation effect can also be observed in a finite slope of the input current waveforms during the rising and falling edges, coinciding with the notches in the corresponding phase voltage. The waveform presented in Figure. 3.5 differ from the voltage waveform, because of notches in the phase voltages. Due to nonzero impedance present in the supply lines produce notches. In the output current waveform, the output current ripple at the 6^{th} multiple of the line frequency can be observed. This ripple slightly disturbs the input current waveforms.

3.2 Nine level DCMLI

In general, the multilevel inverter is preferred to handle medium voltage, current and or power in industries. Diode-clamped MLI requires only one dc source unlike cascaded h bridge inverter, and the voltage balancing

issue is small when compared with flying capacitor multilevel inverter.

The NPC-MLI employs clamping diodes for level making and cascaded DC capacitors for maintaining DC-link voltage. The inverter can usually be configured as a 3-level, 4-level or 5-level topology,but only the3-level NPC-MLI is often called as NPC inverter as it has found wide application in high power applications. The main properties of the NPC inverter include reduced dv/dt and less THD in output voltage. Moreover, the inverter can be used in the ASD to reach a certain voltage level without series switching devices. For instance, the NPC inverter using 6000V devices is suitable for the drives rated at 4160V. In this section, various aspects of the 9-level NPC-MLI are discussed, including the inverter topology, operating principle, and device commutation. Generally, DC input voltage of the inverter is split by four cascaded DC capacitors, providing a floating neutral point 'O' (NP).

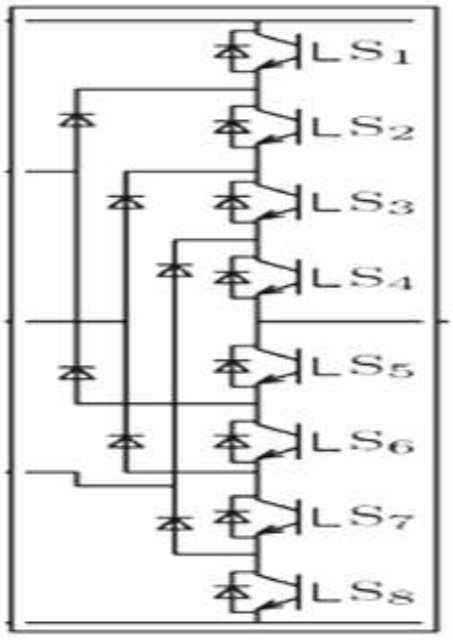

Figure 3.8 Phase A of Nine level DCMLI

Number of power electronic switches per pole = 2(n – 1) (3.43)

Number of DC-link capacitors = (n– 1) (3.44)

Number of clamping diodes per pole =2(n – 2) (3.45)

Voltage across each DC-link capacitor =V_{dc}/ (n-1) (3.46)

Where,

V_{dc} is the DC-link voltage

n is the level of the inverter.

Figure 3.8 shows the simplified circuit diagram of a 9-level NPC-MLI. The leg "A" of an inverter is made out of four active switches $S_1$to S_8 with the anti-parallel diodes. Practically, either the GCT or IGBT can be utilized as a switching device. On the inverter DC side, the DC-bus capacitor is split into four, providing an NP. The diodes connected to the neutral point, are the clamping diodes

The operating status of the switches in the 9-level NPC-MLI can be represented by switching states shown in Table3.2. Switching state,'0' signifies that the upper two switches in leg A are ON and the inverter terminal voltage V_{AN}, which is the voltage at terminal A on the neutral point O, is +E, whereas 'N' indicates that the lower two switches conduct, leading to V_{AN}= (–E). Switching state 'O' signifies that the inner two switches S_{2A} and S_{3A} are ON and V_{AN} is clamped to zero through the clamping diodes. Among the clamping diodes, any one of the clamping diode is turned ON, depending on the direction of load current i_A.For instance, a positive load current (i_A>0) forces D_{1A} to turn ON, and the terminal A is connected to the neutral point O through

the conduction of D_{1A} and S_{2A}

Table 3.2. Switching table for the 9-level NPC-MLI

Device switching Status of PhaseA				**Inverter Terminal Voltage (V_{AN})**
S_1= S_5	**S_2= S_6**	**S_3= S_1**	**S_4= S_8**	
1	1	1	1	E4= V_{dc}
0	1	1	1	E3= $3V_{dc}/4$
0	0	1	1	E2= $V_{dc}/2$
0	0	0	1	E1=$V_{dc}/4$
0	1	0	1	E0=0

.

It can be observed from Table 3.2 that switches S_{1A} and S_{3A}operate in a complementary manner. With one switched ON, the other must be OFF. Similarly, S_{2A} and S_{4A} area complementary pair as well. The gate signal and switching state arrangements, where vg1 to vg4 are the gate signals for S_{1A} to S_{4A}, respectively. The gate signals can be generated by Space Vector Modulation (SVM), Carrier Based Pulse Width Modulation (CBPWM), or Selective Harmonic Elimination (SHE) schemes. The waveform for V_{AN} has three voltage levels, +E, 0 and -E, based on which the inverter is referred to as a 3-level inverter. The inverter terminal voltages V_{AN}, V_{BN}, and V_{CN} are three-phase balanced with a phase shift of $2\pi/3$ between each other. The line to line voltage V_{AB} can be identified from $V_{AB}=V_{AN}-V_{BN}$, which contains five voltage levels (+2E, +E, 0,-E, and -2E).

It can be summarized that all the switching devices present in the NPC inverter withstand only half of the DC-bus voltage during the commutation

from switching state [O] to [P]. Similarly, the same conclusion can be drawn for the commutation from [P] to [O], [N] to [O], or vice versa. Hence, the NPC inverter switches do not have a problem of dynamic voltage sharing. It should be pointed out that the switching between [P]and [N] is prohibited for two reasons:(a) It involves all four switches in an inverter leg, two being turned ON and the other two being commutated OFF, during which the dynamic voltage on each switch may not be kept same. (b) The switching loss is doubled.

3.3 Induction motor drive

Induction Motor is a well-known electrical motor utilized in most applications**.** It can be called as a synchronous motor due to the less speed than synchronous speed. The speed of rotation of the magnetic field is synchronous speed in a rotary machine and it depends upon the number poles of the machine and frequency. Due to the rotation of magnetic field which is produced in the stator will generate flux in the rotor which will make the rotor to rotate, the hence induction motor always runs at speed less than synchronous speed. Due to the lagging of flux current in the rotor with flux current in the stator, the rotor will never reach to its rotating magnetic field speed i.e. the synchronous speed.

3.4 Multicarrier PWM

Waveforms of practical inverters are non sinusoidal and contain higher magnitude of certain lower order harmonics. For low and medium power applications, square wave and quasi-square waveforms may be acceptable, but for high power applications, sinusoidal waveforms with less distortion are required. Harmonic contents present in the output of DC to AC inverters can be eliminated either by using filter circuit or by employing PWM circuits. Use

of filters has the disadvantages of larger unit size, increased losses and hence the reduced efficiency, which results in higher cost for realization, whereas use of PWM techniques reduces the filter requirements to minimum or zero, depending upon the type of applications and the control technique employed for the generation of firing pulses for the power switches and depending upon the type of application. Harmonics are divided into a voltage and current harmonics. A current harmonic are usually generated by the harmonics contained in the voltage supply and depends on the type of load such as resistive load, inductive and capacitive type load. Both harmonics can be generated by either in the load or the source side.

Carrier based PWM methods employs the per carrier cycle volt-second balance principle to program a desirable inverter output voltage waveform. According to this principle, a sequence of inverter states is generated over a carrier cycle in a manner that for each phase the average value of the rectangular pulse output voltage approaches its reference voltage value. In DC-DC converters, the principle has been utilized for a long time. It is normally called as PWM control or duty cycle control. But, its application to three-phase VSIs is not as intuitive as the DC-DC converters. PWM-VSI modulator design and implementation is also substantially more complex than the DC-DC converter duty cycle controllers. This is because, in a three-phase PWM-VSI, the duty cycle of each switch is time variant under both steady state and dynamic operating conditions. Also, the inverter output line to line voltages cannot be independently controlled by any switch,i.e., the VSI is a coupled system.

Therefore, a detailed modulator study requires a knowledge of both macroscopic (over a fundamental cycle) and microscopic (per carrier cycle) behaviour. Following the description of two carriers based PWM implementation techniques, the microscopic and macroscopic views will be

provided. Two main carriers based PWM implementation techniques exist: the direct digital technique and the triangle intersection technique. In the Sinusoidal PWM (SPWM) method, the sinusoidal signal is compared with a triangular carrier signal. The resulting output is used to control the devices of the inverter. Within every carrier cycle, the average value of the output voltage becomes equal to the reference value. Particularly in the digital implementation which employs the regular sampling technique, this result becomes obvious as the reference volt-sec precisely equals the output volt-sec. In the regular sampling technique, output of the positive or negative peak of the triangular carrier cycle and held constant for the remaining of the carrier cycle. Although the early triangle intersection implementations mostly involved analog hardware circuits, the advent of low cost digital electronics rendered the analog solutions obsolete. Most present triangle intersection implementations involve high-resolution digital PWM counters and comparators.

SPWM technique is one of the most famous modulation techniques among the others applied in power switching inverters. In SPWM, a sinusoidal reference voltage waveform is compared with a triangular carrier waveform to produce gate signals for the switches of the inverter. Power dissipation is one of the most important problems in high power applications. To minimize the switching losses, the fundamental frequency SPWM control strategy was proposed. The multi-carrier SPWM control methods also have been implemented to increase the performance of MLIs and have been classified according to vertical or horizontal arrangements of the carrier signal. The vertical carrier distribution techniques are defined as:

- Phase Dissipation (PD)
- Phase Opposition Dissipation (POD)
- Alternative Phase Opposition Dissipation (APOD) and

- Phase shifted (PS)

In phase disposition, all the carriers have same frequency and amplitude. Moreover, all the (n-1) carriers are in phase with each other. In Phase opposition disposition**,** the two carrier waveforms are in phase above or below the zero-reference. However, they are phase shifted by an angle of 180^o between the carrier waveforms above and below the zero-reference.in Alternative phase opposition disposition requires each of the (n-l) carrier waveforms, for an n-level phase waveform, to be phase displaced from each other by 180^o alternatively. In this method, the most significant harmonics are cantered as sidebands around the carrier frequency. It reduces the THD to some extent, nevertheless the output voltage is increased and the voltage stress is reduced. The phase shift technique employs a number of carriers (n-l) phase shifted by 90^o accordingly. In fact PS-PWM is only useful for cascaded H-bridges and flying capacitors, while PD-PWM is more useful for NPC. Hence, PD-PWM used in nine level DCMLI. Each of the above mentioned multi-carrier SPWM control techniques are the most widely used PWM control method due to many advantages including easy implementation, lower harmonic outputs according to other techniques, and low switching losses .

3.5 Modelling of nine level diode clamped multilevel inverter fed induction motor with front end rectifier

Waveforms of practical inverters are non-sinusoidal and contain higher magnitude of certain lower order harmonics. For medium and low power applications, quasi-square and square wave waveforms may be acceptable, but for high power applications, sinusoidal waveforms with lower distortions are required. Harmonic contents present in the output of DC to AC inverters can be eliminated either by using filter circuit or by employing pulse width modulation circuits. Use of filters has the disadvantages of larger unit size,

increased losses and hence the poor efficiency which results in higher cost for realization, whereas use of PWM techniques reduces the filter requirements to minimum or zero, depending upon the type of applications and the control technique employed for the generation of firing pulses for the power switches and depending upon the type of application. Harmonics are divided into a voltage and current harmonics. A current harmonic are usually generated by the harmonics contained in the voltage supply and depends on the type of load such as resistive load, inductive and capacitive type load. Both harmonics can be generated by either load or source side. Traditional two level high-frequency PWM inverters have several problems associated with high-frequency switching, which produces high dv/dt stress across the power switches. While employing the certain control techniques to the multilevel inverters the output voltage harmonics are reduced significantly when compared to the conventional high-frequency PWM techniques. Here the proposed SPWM technique is implemented in PSIM, and the output waveforms were presented for different levels. PSIM is an electronic circuit simulation software package, designed especially for use in power electronic and motor drive simulations .Hence PSIM is more suited and has been adopted for the proposed system simulation and output studies.

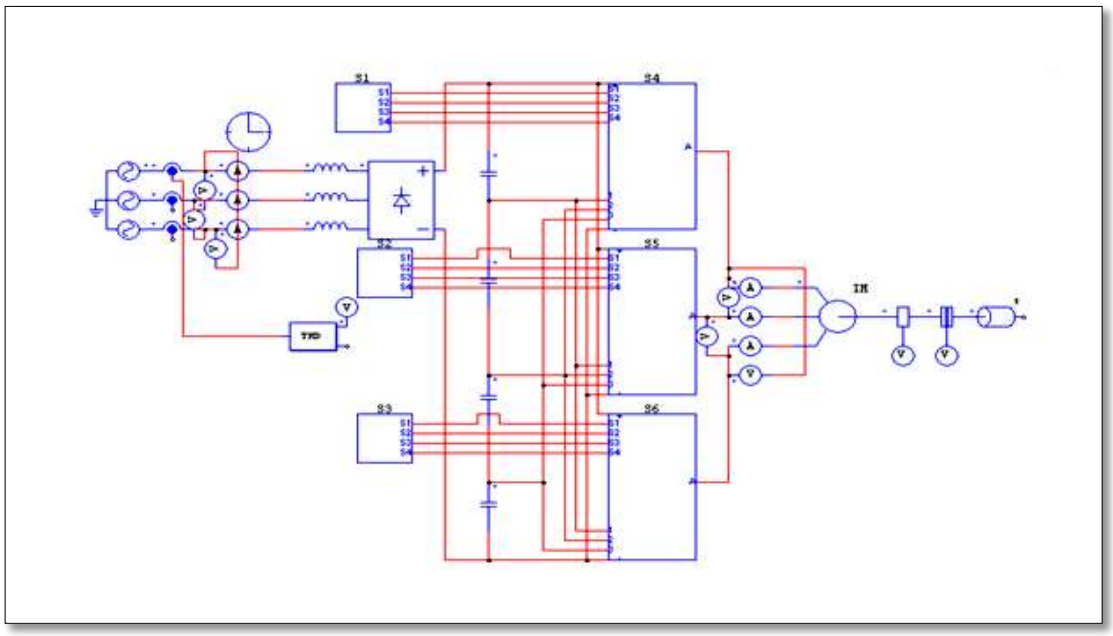

Figure 3.9 PSIM model of nine level diode clamped multilevel inverter fed induction motor with front end rectifier

Figure 3.9 shows the PSIM simulation diagram of nine level diode clamped multilevel inverter fed induction motor with front end rectifier. The circuit constructed using the three phase diode bridge rectifier elements (L, C), three Phase AC source, three phase induction motor, voltage, current THD measurement block with nine level DCMLI. The nine-level DCMLI, is constructed using IGBT and diodes as shown in Figure 3.10 for the sake of convenience, each arm of inverter model is represented as sub-blocks (S4,S5,S6)(S1,S2,S3) are the pulse generating units of the arm of S4,S5,S6 respectively.

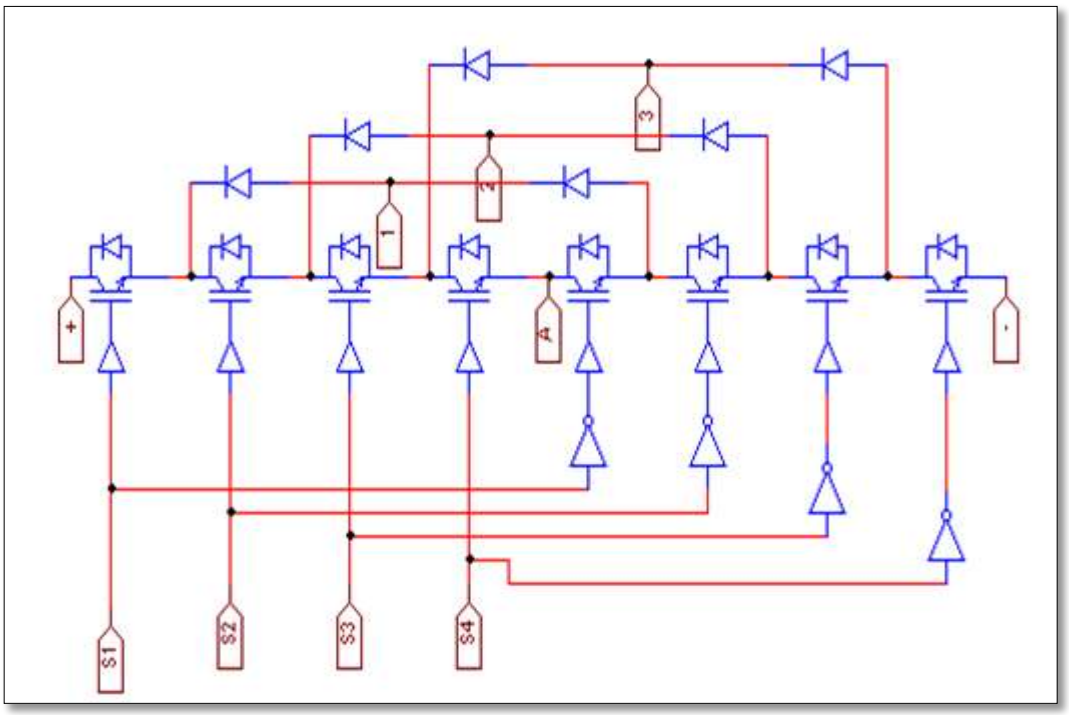

Figure.3.10 Simulation diagram per phase representation used in sub system

Three phase Nine level diode clamped multilevel inverter fed induction motor with front end rectifier is simulated with PSIM software. The sub-block consists of one arm of the nine level DCMLI, where all switches are connected in series with the parallel combination of clamping diodes. The clamping diodes are associated with capacitors, as displayed in Figure 3.9. Switching states of the positive arm is the compliment to the negative arm. So the pulses generated for a positive arm is inverted and fed to the negative arm. PSIM induction motor simulation parameters was tabulated in Table 3.3

Table 3.3 Induction motor simulation parameters

Parameters	Values
R_s(stator)	1.405
L_s(stator)	0.005839
R_r (rotor)	1.395
L_r(rotor)	0.005839
L_m(magnetizing)	0.1722
No of poles	4

The 415V, 50 Hz, AC is used to drive the motor through DC link inverter. The waveform shows per phase voltage waveform and phasor represent 120° displacement. Three phase supply voltage obtained from simulation are shown in Figure. 3.11.

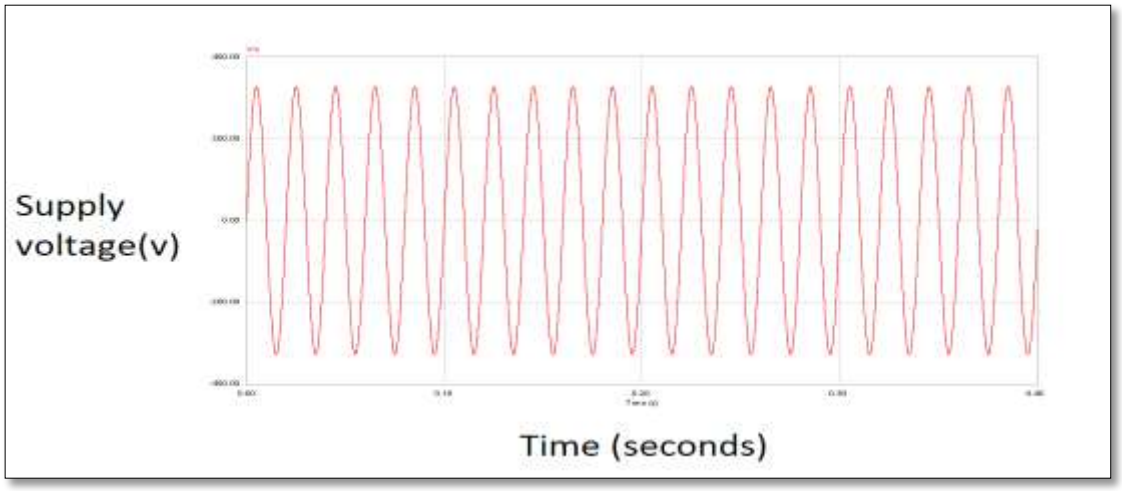

Figure 3.11 Supply voltage 200V/div. Time: 0.10s/div

Figure 3.12 shows a source current under front end rectifier operation. Front end rectifier used in many converter topologies to produce fixed DC output voltage from a fixed AC input voltage. The higher power handling capacity and reduced ripple content are the benefits of six pulse rectifier when compared with single phase rectifier circuit.

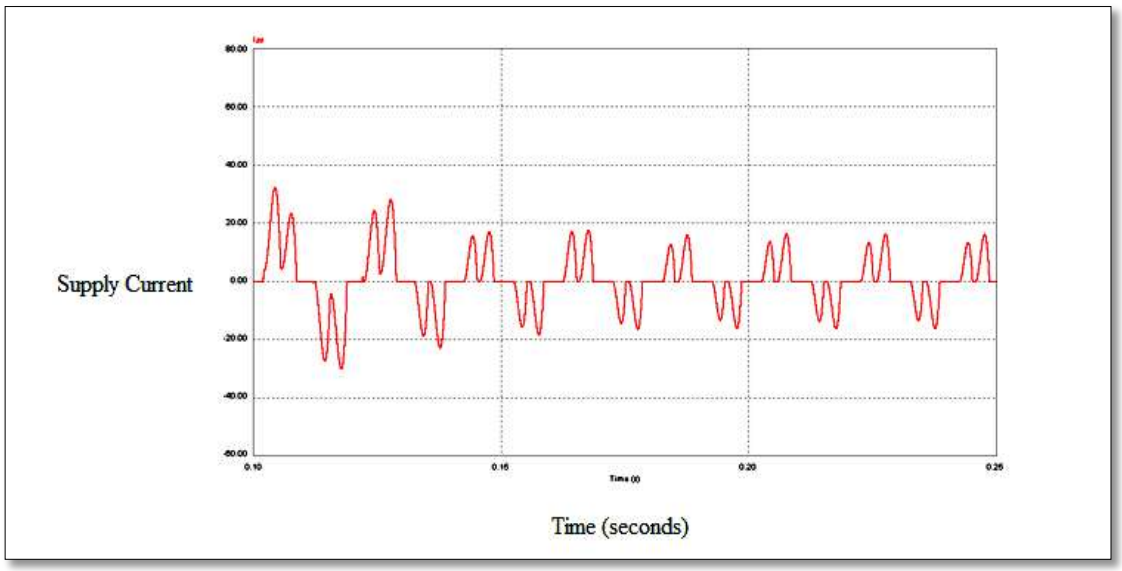

Figure 3.12 Source current 20A/div. Time: 0.15s/div

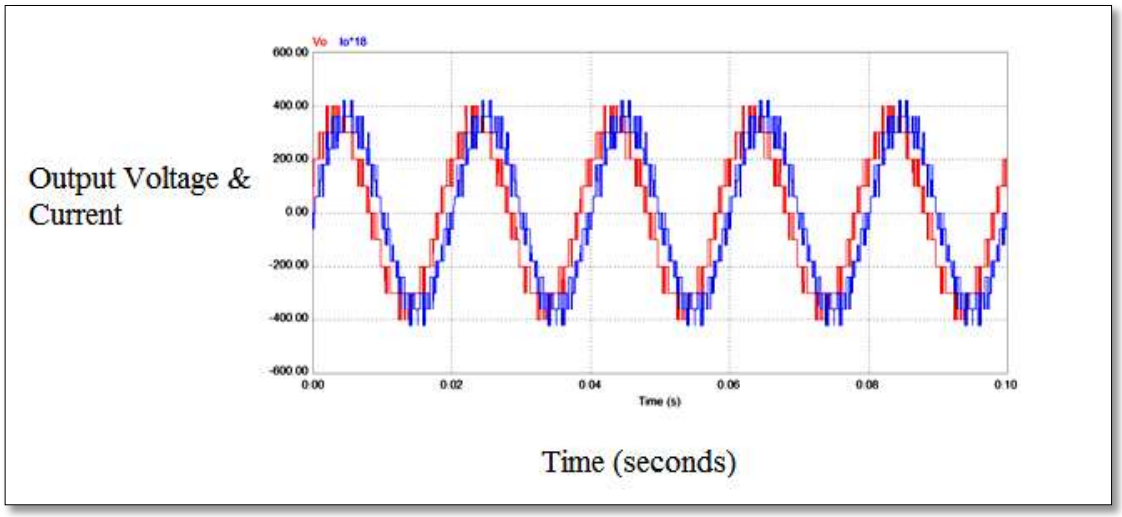

Figure.3.13 Output voltage and current Vo: 200V/div. Io:200A/div(÷18) Time:0.02s/div

The phase ac output voltage and current obtained from simulation are shown in Figure. 3.13. It shows the output voltage, and current of nine levels diode clamped multilevel inverter. The nine levels produce THD about 9%. It is very low when compared with conventional two-level inverter used in adjustable speed drives.

Figure 3.14 shows the value of supply current harmonics and p.f.

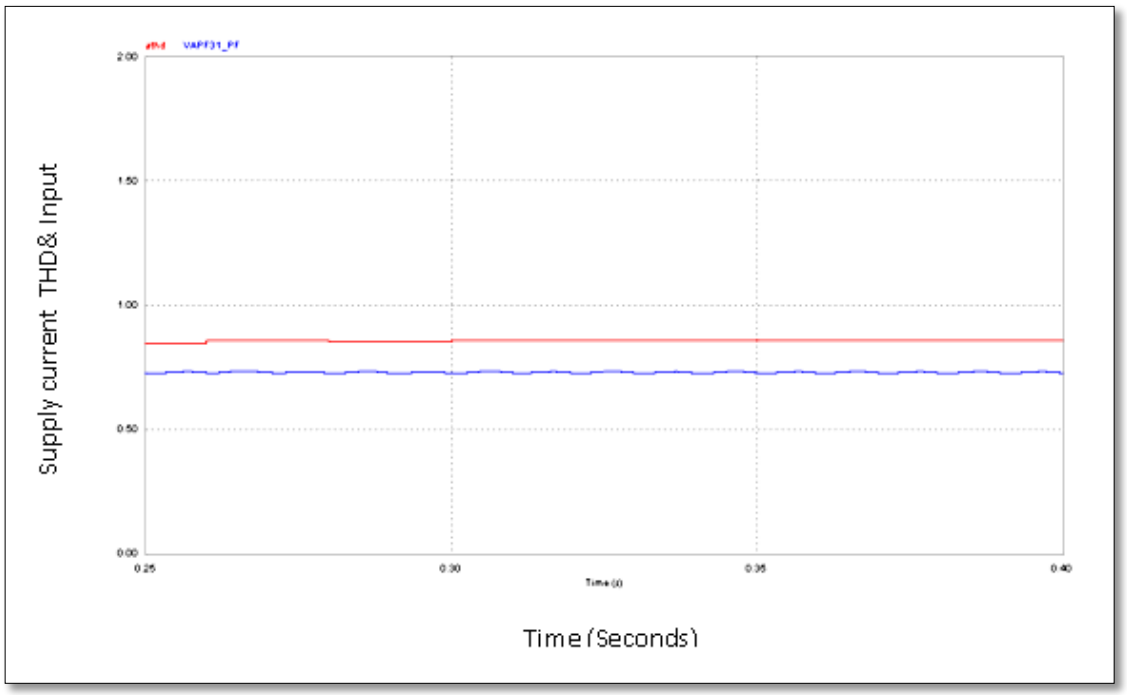

Figure.3.14 THD and PF;athd(THD): 0.2pu/div.
V_APF31_PF(PF):0.2pu/div. Time: 0.05s/div

Unity PF and 0% THD are desirable in DC link inverter. But the typical value of THD and PF of nine level DCMLI is around 85% and 0.73 respectively which is undesirable. It must be improved.

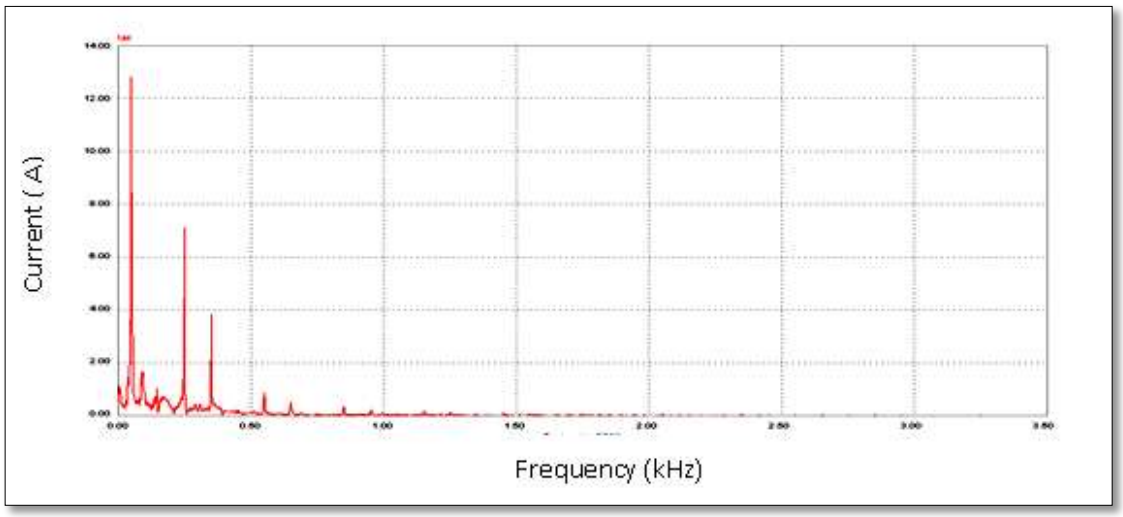

Figure 3.15 FFT spectrum 2.0A/div. Frequency: 0.5kHz/div

The Figure.3.15 shows the FFT spectrum of the supply current as obtained from simulation. It explains the order of harmonics. Waveform clearly shows that the presence of harmonic current. Especially odd order harmonics make an influence on the fundamental components.

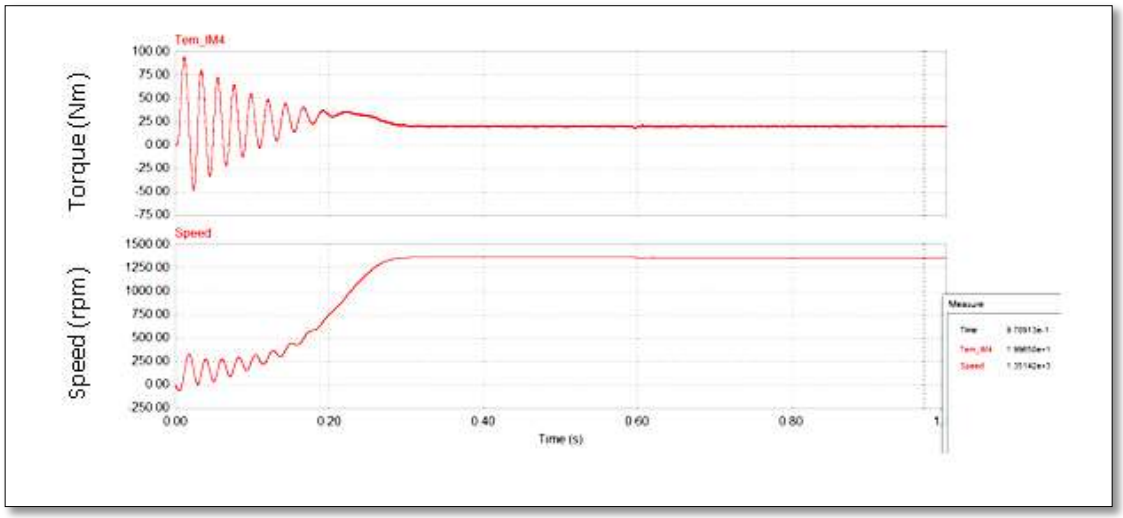

Figure 3.16 Torque and Speed at full load (Simulation)

Tem_IM4(Torque):25Nm/div. Speed: 250rpm/div

The mechanical characteristics of torque and speed of an induction motor obtained from simulation are shown in Figure.3.16.The inverter fed induction motor has smooth speed –torque characteristics. The speed of an induction motor is around 1350 rpm, and it torque developed in the motor is 20 Nm. The torque pulsation is almost zero. The settling time of the given motor drive is about 0.28 sec.

3.6 Summary

The detailed review was done on nine level MLI fed induction motor drive with a front-end rectifier. The performance was analyzed using PSIM simulation software. Various results are obtained, in which the value of THD and PF is 85% and 0.73 (lagging) respectively. The values fail to come to IEEE standards. Simulation results of MLI shows enhanced the harmonic profile of output voltage waveform. It is about 9%. The high-quality voltage used to drive the induction motor. It results in good torque-speed characteristics of the induction motor. Chapter 4 deals with the reduction of the harmonics of the supply current by introducing current injection technique.