CHAPTER 5

NINE LEVEL INVERTER WITH ACTIVE CURRENT INJECTION CIRCUIT

Due to the remarkable progress made in the high power electronic devices, power converters are widely used in industrial applications. In the vast majority of AC-DC power converters, pulse width modulated voltage source inverters supplied from a smooth DC link voltage, are used. This DC link voltage is normally obtained from a 3- phase diode bridge rectifier with a large output capacitor to keep the voltage essentially constant. This is favoured, due to its low cost, simple structure, the absence of control, and robustness. The AC currents, with a capacitive load, contain a high level of harmonics and are discontinuous. Due to the non-linear loads, harmonic currents are increasingly considered to be undesirable, as they penetrate into the supply system and affect the voltage waveforms at the Point of Common Coupling (PCC). This leads to reduced input power factor and increased THD. Therefore, serious power pollution is introduced in the system.

In the passive current injection method, the capacitors and inductors have been used to eliminating current harmonics and enhancing the system power factor. These capacitors and inductors are bulky, costly and sensitive to the line frequency. In addition to they have a narrow input voltage range, occupy a significant area of space, poor dynamic response and they do elimination effectively only for certain harmonic current components. The reactive and resistive component in the passive network decreases the efficiency.

In this chapter, the converter which comprises of HF front-end three-phase diode rectifier and Active Power Factor Correction Circuit (APCC) is

proposed, which overcomes the fore-mentioned disadvantages of the passive compensation. The chapter presents the high-power-factor operation of AC-to-DC converter. The high PF is achieved by injecting HF current, from the HF inverter, at the input of the front- end three-phase rectifier. All the switches of the inverter show zero voltage switching. The diodes of the front- end rectifier works with zero current transition.

The detailed analysis of the converter circuit is presented. With the aid of five different modes on the single phase basis, the operation of the circuit is explained. The experimental and simulation results of 2.5 kW converters are also explained.

5.1 Principle of Operation

An AC-to-DC converter is shown in Figure 5.1 In this converter, the active power factor correction circuit (APFCC) introduced. APFCC increases the power factor by using active electronic circuits with feedback that control the shape of the drawn current.

APFCC constitutes a three-phase inverter (S_1–S_6), inductors (L_a–L_c) and feedback capacitors (C_a–C_c). These elements are designed for high-frequency operation. Therefore, the feedback capacitor gives low impedance for high switching frequency (50 kHz) and it gives a very high impedance to supply (50 Hz). Therefore, the voltage across the capacitor C_a, (v_{Ca}) has modulation at 50 Hz i.e. at any instant the voltage across C_a is equal to the supply voltage, v_a as the capacitor carries high-frequency current, the v_{Ca} has HF voltage ripples superimposed on the power frequency component. Also, these capacitors also provide dc blocking for injected current.

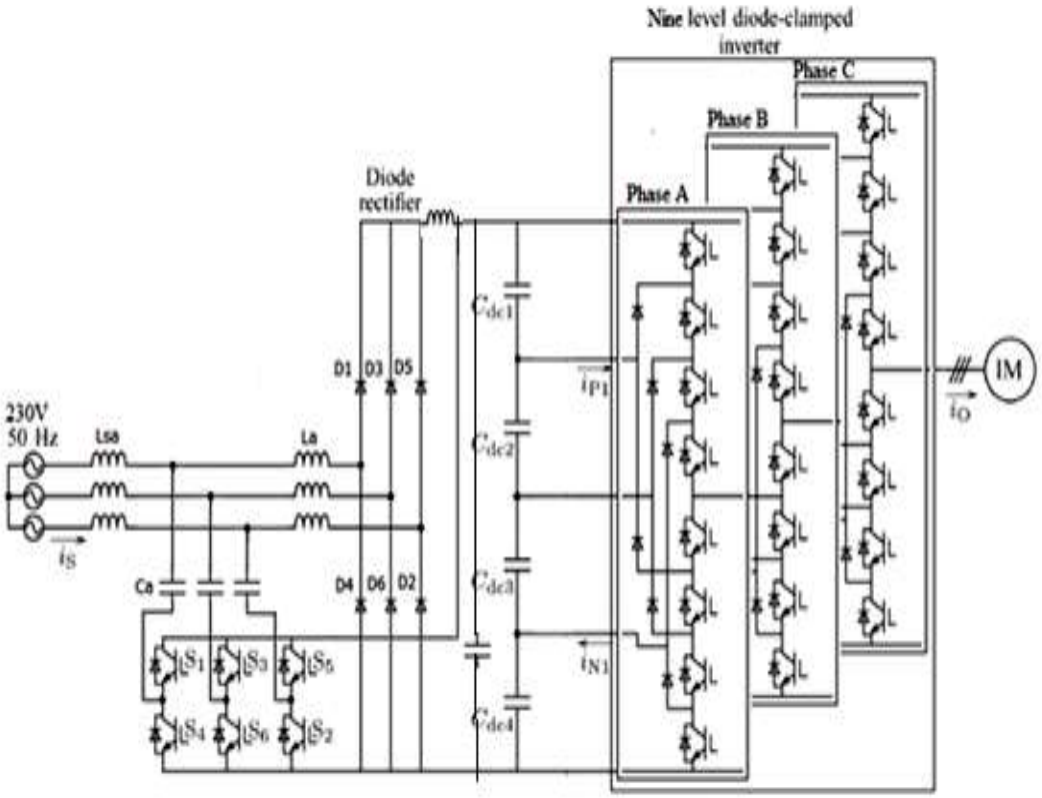

Figure 5.1 PSIM model of DCMLI using a high frequency front-end rectifier and current injection

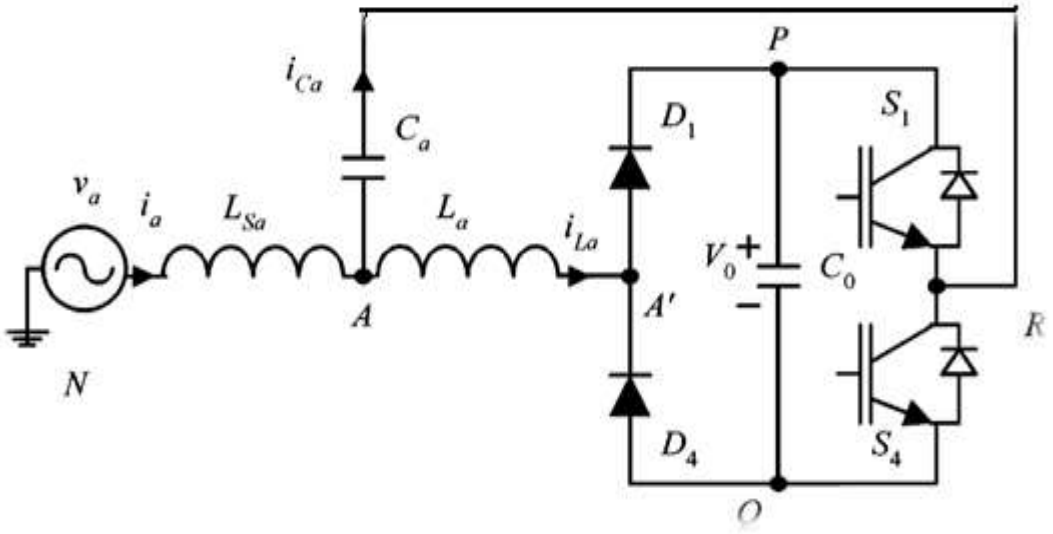

Figure 5.2 Single leg equivalent of phase a

The principle of operation of the converter is best understood by a single-leg equivalent circuit of phase A (Figure.5.2) of the proposed three-phase system. The result of the system can be easily extended to phases B and C also.The switches S_4 and S_1 are switched on and off alternately with a high frequency, f_S. The switching frequency, f_S is very high as compared to the supply frequency f. During a particular switching interval k, when S_1 is on, and S_4 is off voltage appears across L_a, which is same as the supply voltage V_a. During 'ON' period (DT_S), the three inductor currents i_{La}, i_{Lb} and i_{Lc} increase at the rate proportional to the instantaneous values of their respective phase voltages (Figure 5. 3) When S_4 is on, the voltage applied across inductor L_a is ($V_a - V_o$) and current, i_{La} decreases to zero at the end of period T_d. The maximum current value, I_{Lap} during ON period, in a particular switching cycle varies with input source voltage.

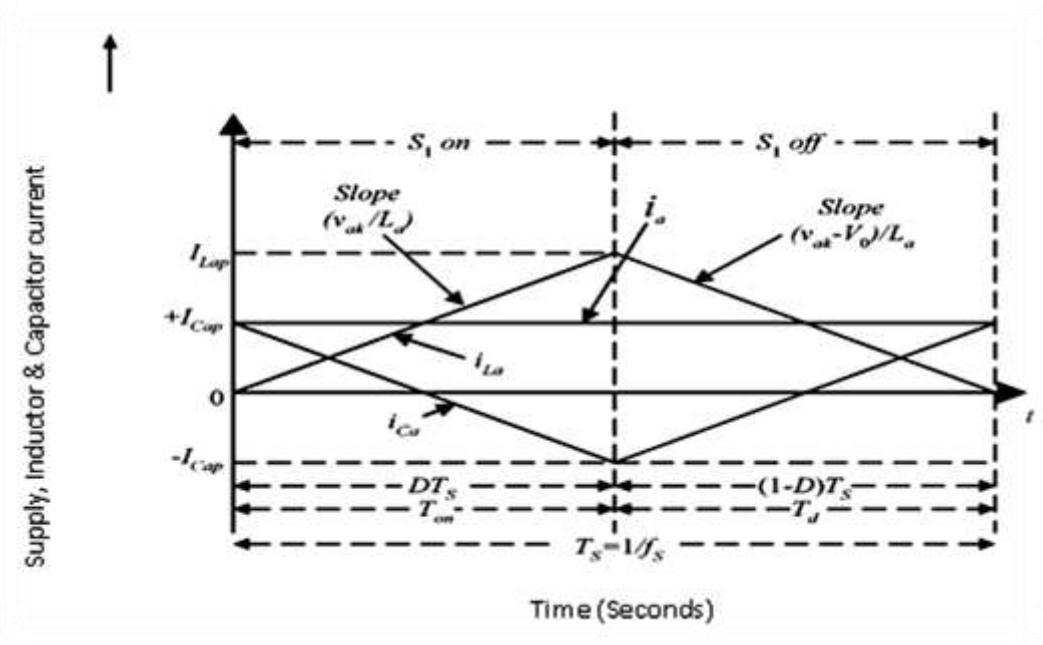

Figure 5. 3. Idealized supply current (i_a), inductor current (i_{La}) and capacitor current (i_{Ca}) in a switching cycle.

Hence, the inductor current, I_{Lap} vary sinusoidally in the envelope determined by supply phase voltage (Figure 5. 4). The supply current is the addition of average values of i_{La}, i_{Ca} and $i_{La(avg)}$, ($i_{Ca(avg)}$).The $i_{Ca(avg)}$, over a switching cycle is zero.

5.2 Design of Current Injection

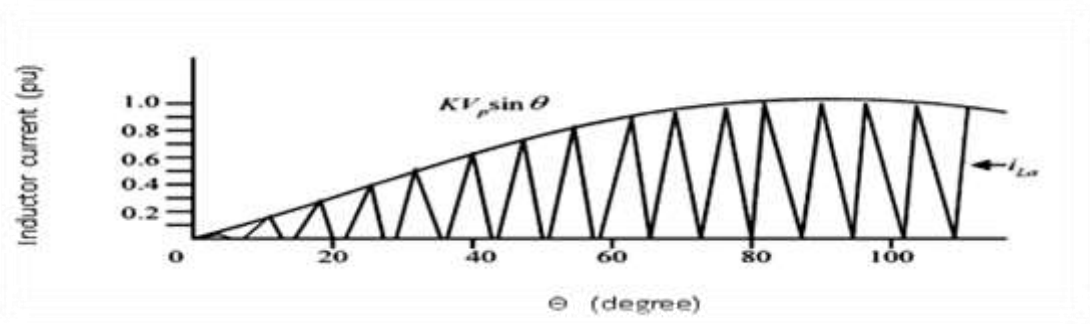

Figure 5.4. Inductor current(i_{La}) with the envelope of a supply voltage

Hence, supply current peaks also vary sinusoidally. Further more, since the inductor current pulses always begin at zero, their average values also vary sinusoidally (Figure. 5.5) almost in phase with the supply voltage.

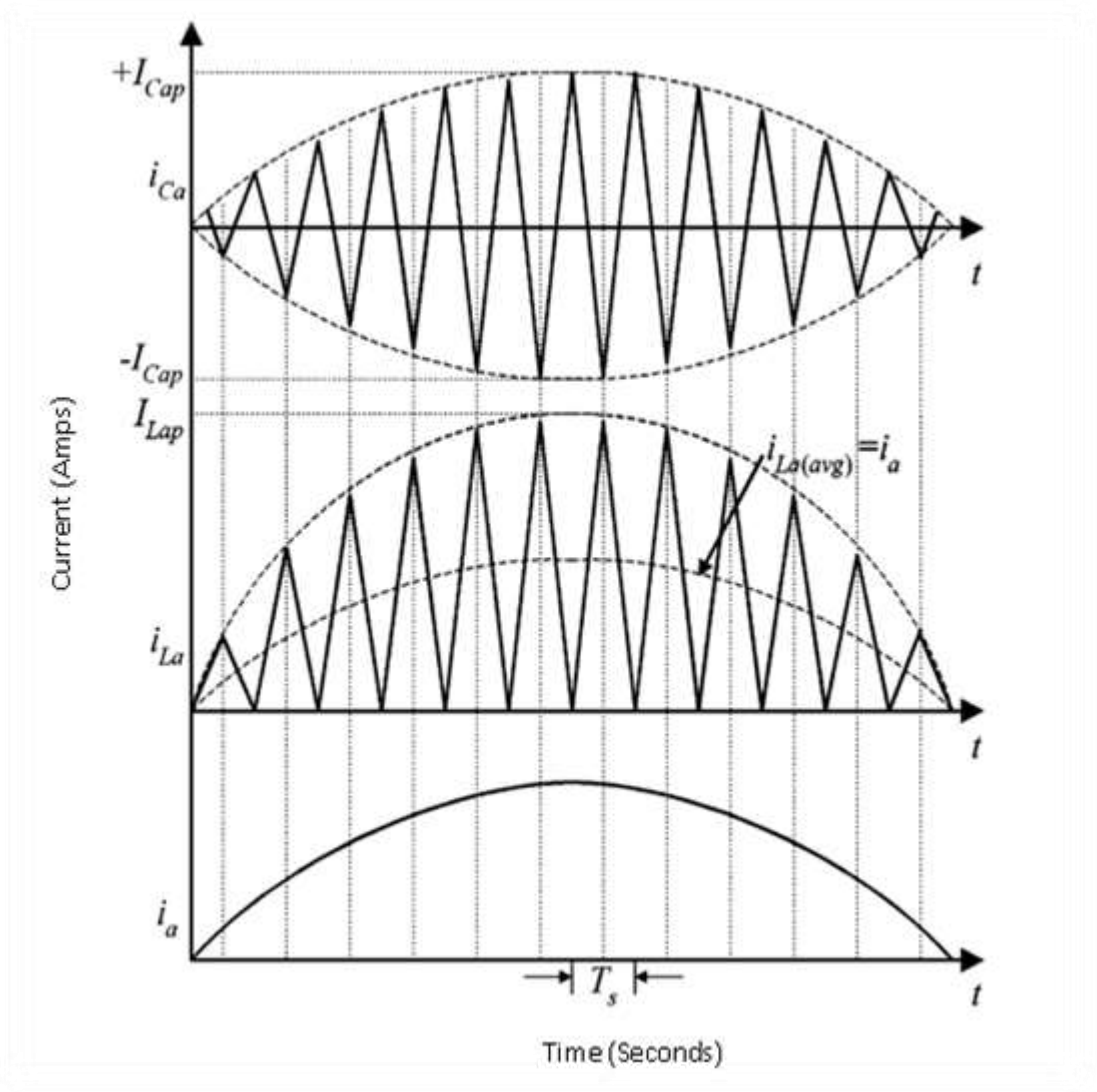

Figure 5.5.Idealized supply current (i_a), inductor current (i_{La}), and capacitor current (i_{Ca})in a half cycle of a supply voltage.

The same action is taking place in other phases and a negative cycle of the supply voltage also. Therefore, the overall power factor is very close to unity. The HF switching of inductor forces diodes of the three-phase rectifier (D_{S1}, D_{S4}, D_1) to turn off and turn on at the switching frequency during the complete cycle of the supply voltage, including the region around zero-crossing (valley points) of a supply voltage. When none of the diodes are conducting, line current flows through the capacitor (C_a –C_c) and inverter switches (S_1 –S_6). Thus, maintains the continuous current through the source inductor. This

removes the discontinuity in the supply current and hence source inductor (L_{Sa} –L_{Sc}) works in continuous conduction mode (CCM). The operation of source inductance in CCM leads to the inherent enhancement of the input power factor. In a switching cycle, even for unbalanced input supply voltages, the supply current (i_a) varies with the amplitude of the supply voltage (v_a) of the particular phase. The i_a always follow the v_a and varies in a sinusoidal envelope over a power frequency cycle and remains in phase (Figure 5.5) irrespective of the unbalance or balance voltage, maintaining high-power-factor. Thus, active wave shaping of the input current waveform and operation at high-power-factor is obtained through APFCC.

As the switching frequency is very high, the input supply current is given by (5.1)

$$i_a = i_{La\,(avg)} + i_{Ca(avg)} \tag{5.1}$$

Where

i_a is line current of phase a,

$i_{La(avg)}$ is average currents through inductor L_a

$i_{Ca(avg)}$ is average currents through dc blocking capacitor C_a

When switch S_1 is turned on, during the positive cycle of supply voltage, the current i_{La} increases linearly from zero to peak value of inductor current, I_{Lap} (Figure. 5.3), whereas, the current i_{Ca} (through C_a), at the same time, decreases linearly from positive peak ($+I_{Cap}$) to zero and then to negative peak ($-I_{Cap}$). When S_4 is on, i_{La} starts decreasing from its peak value to zero. The i_{Ca} starts increasing from $-I_{Cap}$ to + I_{Cap} through zero, maintaining almost constant i_a, during a switching cycle. It is to be noted that, when none of the diodes is conducting, i_{La} is zero but a (non-zero) flows through C_a and the inverter. Thus discontinuity in the supply current, which is mainly responsible for deteriorating the quality of the supply current and power factor, is removed

thereby leading to high PF operation of the circuit.

All the inverter switches operate with Zero Voltage Switching (ZVS).The current i_{Ca} was flowing through S_4, switch S_4 is turned off. It flows through the body of the diode (D_{S1}) switch S_1.Therefore, the voltage across the switch $S_1$is almost zero. Meantime, when the gate pulse is supplied to switch S_1, the current through D_{S1}decreases to ”0” and S_1 starts conducting the current in the forward direction with almost “0” voltage across it. Hence, S_1 operates with ZVS. In the same way, when switch S_1 is turned off, the current which was flowing through it, flows through the body diode (D_{S4}) of switch S4. Therefore, the voltage across the switch S_4 is almost zero. When the gate pulse is supplied to it then, it starts conducting the current through it at almost zero voltage across it. Hence, S_4 also operates with ZVS. Thus switches operate with ZVS. The diodes of the front-end rectifier show zero current transition (ZCT). The diode conducts almost for a complete switching cycle except for a small period. The diode current falls to"0" and then the voltage across it rises. As the current through the diode (D_1) and the inductor (L_a) are same, the diode current falls to zero when the inductor completely releases its energy. The active wave shaping of the input current waveform is obtained by the use of HF injected current from HF inverter, the capacitor (C_a –C_c) and inductor (L_a –L_c).

The actual value of output DC voltage, V_0 is fed to DSP (TMS320F2812) through low pass filters (LPF). This actual value, V_0 is then compared with reference values in the DSP. Accordingly switching frequency is changed. The event managers (A and B) present in the DSP are programmed to generate PWM pulses. The software is developed to generate the PWM pulses, with a proper dead band to avoid shoot-through fault. These pulses are made present on the pins PWM1, PWM2, PWM3, PWM4, PWM5, and PWM6. These PWM pulses are fed to the logic driver and isolator for proper

level shifting and isolation. The bipolar gate driver (PC817) circuit is used to drive the IGBTs, because it has a high isolation voltage between input and output. The bipolar pulses also help to ensure the fast and reliable turn-off of the IGBTs. Since switching frequency is very high, filtering of the unwanted input current harmonics becomes easier with a small source inductor.

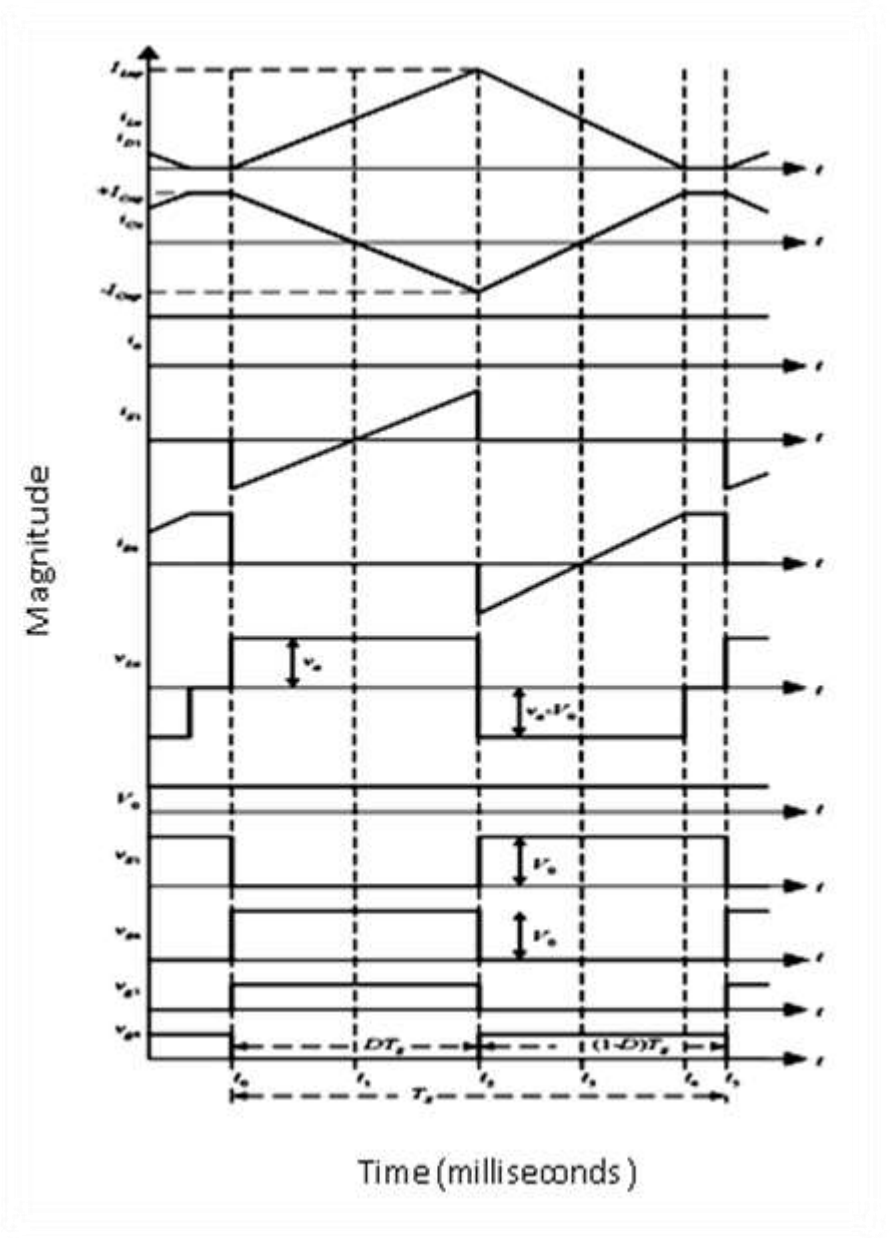

Figure 5.6.Different modes of key wave forms

Five different modes of operation of the circuit are explained. As the working with the three-phase circuit is complex, for the ease of understanding, modes are present, considering single-phase system. An operation is considered as the peak of input supply voltage v_a since the maximum voltage, and current stresses occur at this instant.

5.2.1 Mode-I (t_0 –t_1)

Mode-I begins at t = t_0. Theoretical key waveforms are depicted in Figure 5.6. The equivalent circuit for this mode is given in Figure. 5.7 Before the commencement of mode -I, switches S_4, S_5, and S_6 were conducting. At t_0 , S_4 is turned off, i_{Ca}, which was flowing through S_4 now flows through D_{S1} , a body diode of S_1 . The voltage across S_1 is almost zero. Hence, zero voltage-switching (ZVS) is achieved when the gating signal is applied to S_1 at this instant. S_5 continues to remain on in the interval (t_0 –t_1). At t_0 ,i_{La} , the current through the inductor L_a ramps up linearly. The i_{La} is given by

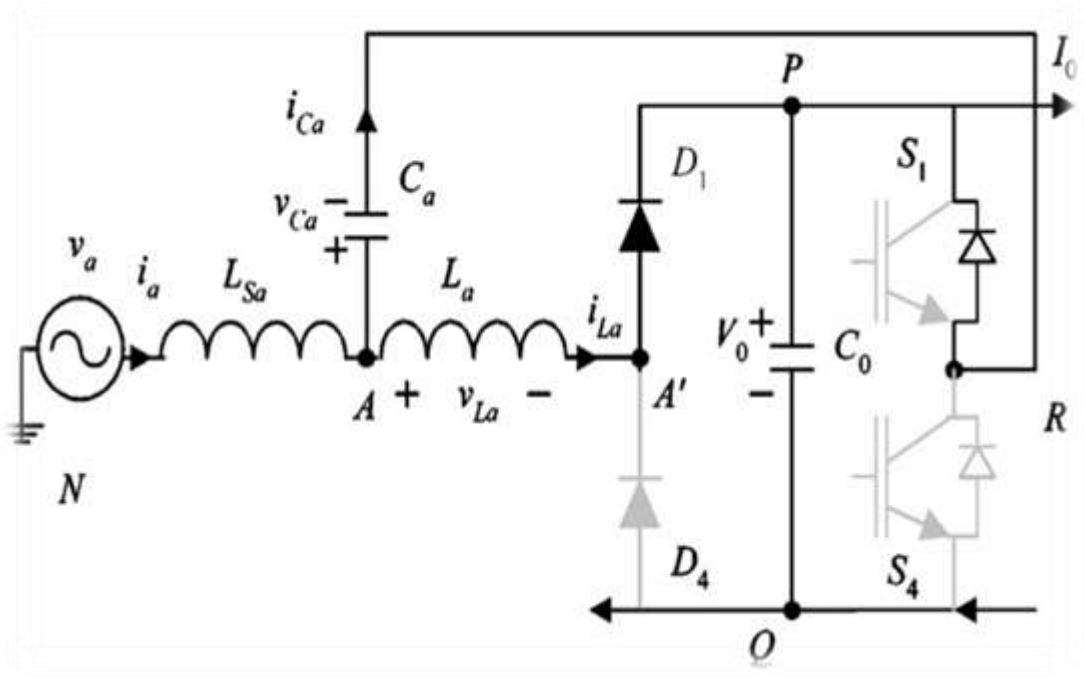

Figure 5.7 Operating mode I

$$L\,\frac{di_{La}}{dt} - v_{ca} = 0 \quad \text{and} \quad v_{ca} = v_a \tag{5.2}$$

$$i_{La(t)} = \frac{v_a}{L_a}(t - t_o) \tag{5.3}$$

The current through capacitor Ca is given by 5.4

$$i_{ca(t)} = I_{cap} - C_a\,\frac{dV_a}{dt} \tag{5.4}$$

Where

I_{cap} is the positive peak value of capacitor current at the start of the model –I at $t=t_o$

At the end of the interval, at $t=t_1$, i_{ca} is zero.

The supply current through rectifier diode D_1, at the end of the mode I is as per (5)

$$i_{a(t1)} = I_{La(t1)} \tag{5.5}$$

The inductor current at the end of mode I is given by (5.6)

$$i_{La(t1)} = \frac{v_a}{L_a}(t_1 - t_0) \tag{5.6}$$

The supply current at the end of this mode I is given by (5.7)

$$i_{a(t1)} = i_{La(t1)} + i_{ca(t1)} \tag{5.7}$$

The current through the capacitor c_a, i_{ca} decreases from its positive peak, $+I_{ca}$ to 0 at the end of the interval at $t=t_o$. During the interval D_{S1}, S_5, S_6, D_1 and D_6 devices conduct.

5.2.2 Mode-II (t_1–t_2)

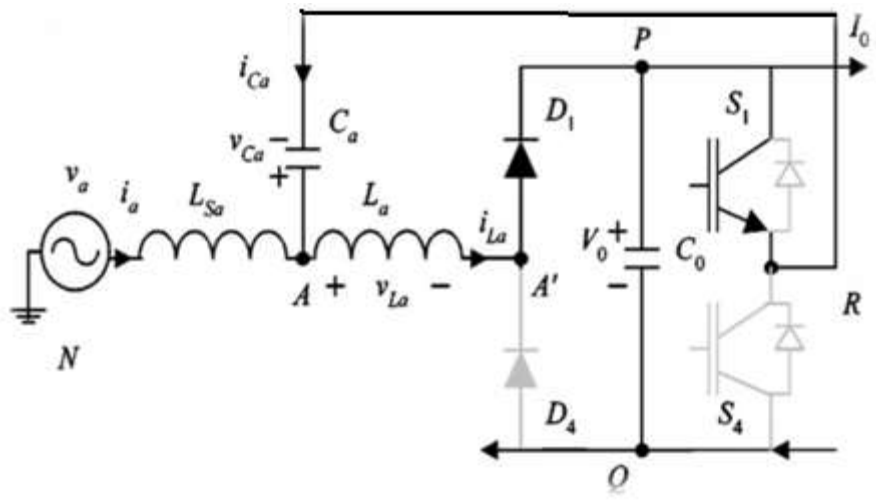

Figure 5.8 Operating mode II

The equivalent circuit for this mode is shown in Figure. 5.8 In this mode i_{La} increases from its previous value $i_{La(t1)}$ and reaches to peak value I_{Lap} and i_{Ca} reach to a negative peak, $-I_{Cap}$. The equations governing this mode are

$$i_{La(t)} = i_{La(t_1)} + \frac{v_a}{L_a}(t - t_1) \qquad (5.8)$$

At $t=t_2$, $i_{La}= I_{Lap}$

therefore,(5.8) can be written as

$$I_{Lap=}i_{La(t_1)} + \frac{v_a}{L_a}(t_2 - t_1) \qquad (5.\ 9)$$

From equation (5.6) and (5.9)

$$i_{La(t)} = \frac{v_a}{L_a} t_{02} = \frac{v_a}{L_a}(DT_S) \qquad (5.\ 10)$$

$$i_{Ca(t)} = -C_a \frac{v_a}{(t-t_1)} \qquad (5.11)$$

The supply current at the end this mode is given by (5.12)

$$i_{a(t_2)} = \frac{I_{Lap}}{2} \qquad (5.\ 12)$$

5.2.3 Mode-III (t_2–t_3)

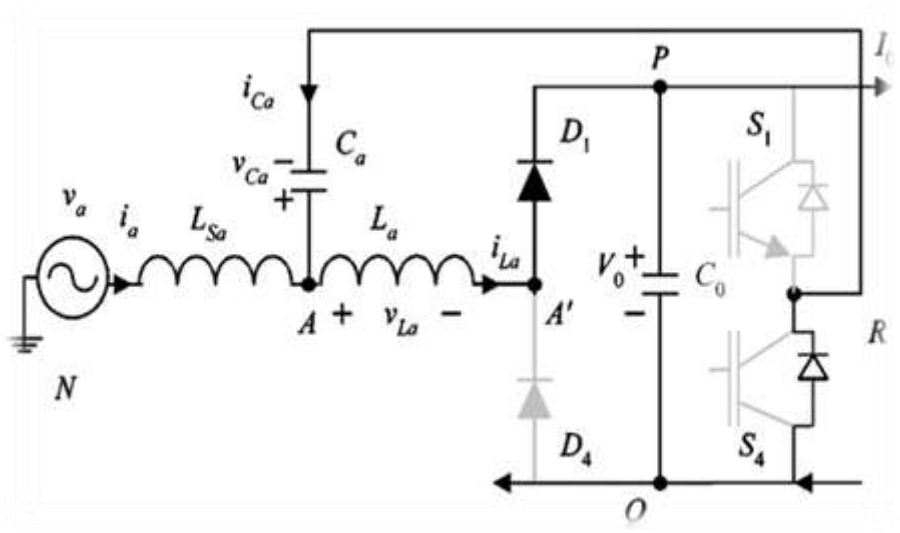

Figure 5.9 Operating mode III

At the start of this mode Figure. 5.9, S_4 is gated, the current through S_1 (i_{S1}) reduces to "0" and the body diode of S_4, D_{S4} conducts. If S_4 is gated during this interval, then ZVS is achieved. The current through S_4 increases linearly, i_{Ca} reaches to zero and i_{La} ramps down to supply current in that interval, i_a. Associated equations during the mode are as follows:

$$i_{La(t)} = I_{Lap} - (V_O - v_a)\left(\frac{t-t_2}{L_a}\right) \quad (5.13)$$

$$i_{Ca(t)} = -I_{Cap} + C_a\left(\frac{V_a}{t-t_2}\right) \quad (5.14)$$

At the end of mode-III, $t = t_3$, $i_{Ca} = 0$

The supply current at the end of mode-III is

$$i_{a(t3)} = i_{La(t3)} \quad (5.15)$$

5.2.4 Mode-IV (t_3–t_4)

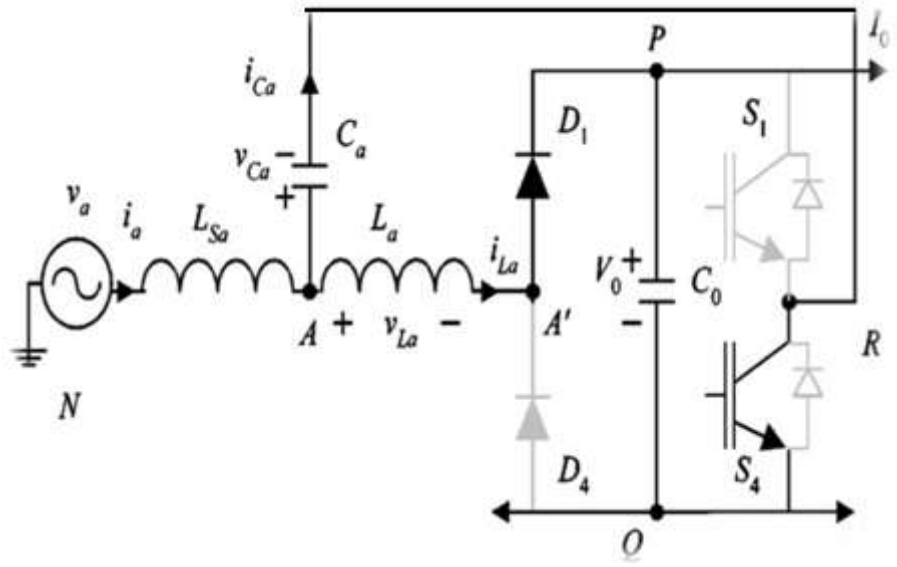

Figure 5.10 Operating Mode IV

The equivalent circuit for this mode is shown in Figure. 5.10.During this interval i_{Ca} increases and i_{La} decreases. At the end of this interval i_{Ca} ramps to $+I_{Cap}$ (same as supply current), and i_{La} to zero. Different equations governing this mode are given below:

$$i_{Ca(t)} = C_a\left(\frac{v_a}{t-t_3}\right) \quad (5.16)$$

$$I_{Cap} = C_a\frac{v_a}{t_{34}} \quad (5.17)$$

$$i_{La(t)} = i_{La(t3)-}\left(\frac{V_O - v_a}{L_a}\right)(t - t_3) \quad (5.18)$$

At the end of the interval, i_{La} is zero. Therefore, from (5.18)

$$i_{La(t3)-}\left(\frac{V_O - v_a}{L_a}\right)(t_4 - t_3) \quad (5.19)$$

5.2.5 Mode-V (t_4–t_5)

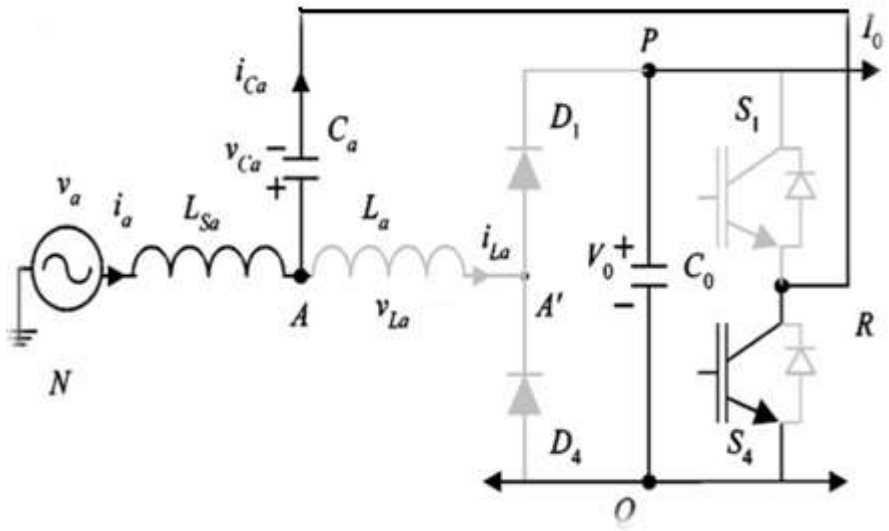

Figure 5.11 Operating mode V

In this interval neither D_1 nor D_4 conducts. In traditional rectifier, this produces the discontinuity in the supply current and mainly responsible for harmonics and reduced power factor. It is to be noted that, in this mode, though diodes do not conduct, still the line current is continuous as it is carried by capacitor C_a. Therefore, line current i_a flows (without discontinuity) maintaining high-power factor. Figure.5.11 depicts the equivalent circuit for this mode. Following equations are valid during mode-V

$$i_{La(t)} = 0 \tag{5.20}$$

$$i_{Ca(t)} = i_{Cap} = i_a \tag{5.21}$$

In summary, from t_0 to t_2, when S_1 is on (S_4 off) current i_{La} increases from 0 to $+I_{Lap}$ and i_{Ca} decreases from $+I_{Cap}$ to $-I_{cap}$ through 0. When S_4 is on (S_1 off), i_{La} ramps down to zero from $+I_{Lap}$ in t_2–t_4 and i_{Cap} increases from $-I_{Cap}$ to $+I_{Cap}$ through 0 and held constant at $+I_{Cap}$ during t_4–t_5.

5.3 Analysis

To simplify the analysis following assumptions are made,

- Input three-phase supply is purely sinusoidal and balanced.
- The power line frequency (50Hz) is far lesser than switching frequency (50KHz)(f_S>f).
- Output filter capacitance is large enough (40nF).so that the output voltage can be considered as constant over a half power cycle period.
- All the switches and components are considered to be ideal. The three-phase voltages are given by

$$v_R = V_P \sin(\omega t), v_Y = V_P \sin(\omega t - \frac{2\pi}{3}), v_B = V_P \sin(\omega t + \frac{2\pi}{3}) \quad (5.22)$$

5.3.1 Input supply current, i_a

Since the switching frequency is very high, the AC line currently in a switching period, as stated earlier, is the sum of average values of i_{L1} and i_{C1}. Therefore,

$$i_R = i_{La(avg)} + i_{Ca(avg)} \quad (5.23)$$

$$i_{La(avg)} = \frac{1}{T_s}\left[\int_0^{T_{s/2}} \left(\frac{I_{Lap}}{T_s} t\right) dt + \int_{T_{s/2}}^{T_s} (T_s - t)\, dt = \frac{I_{Lap}}{2}\right. \quad (5.24)$$

From equation (5.10),(5.19) and (5.24)

$$i_{La(avg)} = \frac{DT_S v_R}{2L_a} \sin \omega t \quad (5.25)$$

Where,

V_p is peak value of input phase voltage,

D is duty cycle of switching period.

Similarly, average value of capacitor current, i_{Ca} can be given as,

$$i_{La(avg)} = \frac{1}{T_s}\left[\int_0^{T_{s/2}} \left(-\frac{4I_{Lap}}{T_s} t + I_{Cap}\right) dt + \int_{T_{s/2}}^{T_s} \left(\frac{4I_{Lap}}{T_s} t - 2I_{Cap}\right) dt = 0\right. \quad (5.26)$$

Therefore, average capacitor current during a switching period is zero.

Equations. (5.21), (5.23) and (5.26) lead to

$$i_a = \frac{DT_S V_P}{2L_a} \sin \omega t = KV_P \sin \omega t \quad (5.27)$$

Where,

$$k = \frac{DT_S}{2L_a}$$

Equation. (5.27) Clearly reveals that the input supply current i_a, is always in phase with the supply voltage, v_a. Hence the proposed converter operates at unity power factor.

5.3.2 Output dc voltage, V_0

To have almost constant dc voltage V_0, at the output of rectifier, generally large capacitor, C_0 is connected. This acts as the input voltage to HF inverter. From Figure.5.10and Equation 5.13, the current in the interval, T_d (discharge time), when S4 is on, is given by

$$i_{La(t)} = I_{Lap} - (\frac{v_o - v_a}{L_a})T_d \quad (5.28)$$

But at the end of the interval, $i_{La} = 0$. Therefore from (5.28)

$$I_{Lap} = (\frac{v_o - v_a}{L_a})T_d \quad (5.29)$$

From (5.10) and (5.29) duty cycle D is given by (5.30)

$$D = \frac{v_o - v_a}{L_a} \quad (5.30)$$

At the peak of a supply voltage, $v_a = V_p$ and t_{on} and t_d periods are equal.

Therefore, from Equation. (5.30), the DC output voltage is given by

$$V_0 = 2V_p \quad (5.31)$$

5.3.3 Power factor and THD

From Equations. (5.27) and (5.30)

$$i_a = \frac{D^2 T_S}{2L_a} v_a \left(\frac{v_0}{v_0 - v_a}\right) = \frac{D^2 T_S}{2L_a} v_a \left(\frac{\beta \sin \omega t}{1 - \beta \sin \omega t}\right) \quad (5.32)$$

Where,

$\beta = V_p/V_0$,a constant

The power factor can be defined as the ratio of real input power, P to the product of input rms voltage, V_{arms} and input rms current I_{arms}

$$P = \frac{1}{\pi}\int_0^{\pi} v_a i_a d\omega t = \frac{1}{\pi}\int_0^{\pi} v_p \sin \omega t \gamma \beta \frac{\sin \omega t}{1 - \beta \sin \omega t} d\omega t \quad (5.33)$$

$$P = \frac{1}{\pi} V_P \gamma \beta \frac{u}{\pi}$$

Where,

$$\gamma = \frac{D^2 T_S V_0}{2L_a} v_a$$

$$u = \int_0^{\pi} \frac{\sin^2 \omega t}{1 - \beta \sin \omega t} d\omega t = -\frac{2}{\beta} - \frac{\pi}{\beta^2} + \frac{2}{\beta^2 \sqrt{1-\beta^2}}\left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-\beta}{\sqrt{1-\beta^2}}\right)\right] \quad (5.34)$$

The input rms current, I_a is

$$I_a = \left\{\frac{1}{\pi}\int_0^{\pi} {i_a}^2 d\omega t\right\}^{\frac{1}{2}} = \left\{\frac{1}{\pi}\int_0^{\pi} \left[\gamma \beta \frac{\sin \omega t}{1 - \beta \sin \omega t}\right]^2 d\omega t\right\}^{\frac{1}{2}} \quad (5.35)$$

$$I_a = \gamma \beta \frac{\sqrt{x}}{\sqrt{\pi}}$$

Where x is defined

$$x = \frac{2}{\beta(1-\beta^2)} + \frac{\pi}{\beta^2} + \frac{2\beta^2 - 1}{\beta^2(1-\beta^2)} \frac{2}{\sqrt{(1-\beta^2}} \left[\frac{\pi}{2} - \tan^{-1}\left(\frac{-\beta}{\sqrt{(1-\beta^2}}\right)\right] \quad (5.36)$$

Therefore, power factor (PF) is given as

$$PF = \frac{P}{V_a I_a} = \frac{\sqrt{2}}{\sqrt{\pi}} \frac{u}{\sqrt{x}} \quad (5.37)$$

The total harmonic distortion (THD) is given by Equation. (5.38)

$$\text{THD} = \frac{1}{\text{PF}}\sqrt{1 - \text{PF}^2} = \sqrt{\frac{\pi x - 2u^2}{2u^2}} \tag{5.38}$$

5.3.4 Design of inductor, L_a

During ON period, the voltage across L_a is v_a and $V_0 - V_a$ during the discharge period. As one moves towards the peak of the supply voltage from valley points, the forcing function $V_0 - V_a$ decreases. At the peak of the supply voltage, it has the least value, and in effect, discharge time may be too long. From the design point of view, L_a should be such that the current through it is just continuous at the beginning of the next cycle. Therefore, $T_d \leq t_{on}$. Three-phase input power is given by

$$P = 3V_aI_a \tag{5.39}$$

At the peak of input phase voltage,

$$i_a = I_p = \frac{I_{Lap}}{2}(I_p - \text{ peak value of } i_a) \tag{5.40}$$

From equations 5.29, 5.39 and 5.40

$$L_a = \frac{3}{4}\frac{(1-D)T_s{V_p}^2}{P} = \frac{3}{4}\frac{(1-D)\,{v_p}^2}{f_sP} \tag{5.41}$$

5.3.5 Design of capacitor, C_a

In a switching cycle current through the capacitor is given by

$$i_{ca} = \left(-\frac{4I_{cap}}{T_S}t + I_{cap}\right) \tag{5.42}$$

The average value of this current is zero. The rms value, I_{Ca} is given by

$$I_{ca} = \left(\frac{1}{(T_s/2)}\int_0^{\frac{T_s}{2}}\left(-\frac{4I_{cap}}{T_S}t + I_{cap}\right)^2 dt\right)^{\frac{1}{2}} = \frac{I_{cap}}{\sqrt{3}} \tag{5.43}$$

At the peak of supply, peak value of capacitor current and supply current is equal. Therefore,

$$I_{ca} = \frac{I_p}{\sqrt{3}} \tag{5.44}$$

Energy stored in the capacitor is given by

$$\frac{1}{2} C_a {V_{ca}}^2 = V_{ca} I_{ca} T_s \tag{5.45}$$

From (5.39), (5.40) and (5.45), the value of capacitor is given by (5.46)

$$c_a = \frac{4\sqrt{2} T_s P}{3\sqrt{3} {V_p}^2} = \sqrt{\frac{32}{27}} \frac{P_0}{{V_p}^2 f_s \eta} \tag{5.46}$$

Where,

f_S is switching frequency,

P_0 is output power

$\boldsymbol{\eta}$ is efficiency of the converter

5.4 Results and Discussion

Three phase nine level DCMLI fed induction motor with front end rectifier and active network compensation is simulated with PSIM software. The sub-block consists of one arm of the nine levels DCMLI, where all switches are connected in series with the parallel combination of clamping diodes. The clamping diodes are joined with capacitors, as shown in Figure 5.12. Switching states of a positive arm are complimentary to the negative arm. Hence, the pulses generated for a positive arm is inverted and fed to the negative arm. Three phase nine levels DCMLI fed induction motor with active current injection is studied. The active current injection network is made up of resonating components and six IGBT switches. It improves the system performance. It limits the size of resonating components and the related losses (inverter switching loss, diode bridge conduction loss, gate control circuit

losses and losses in parasitic elements). It offers a better dynamic response.

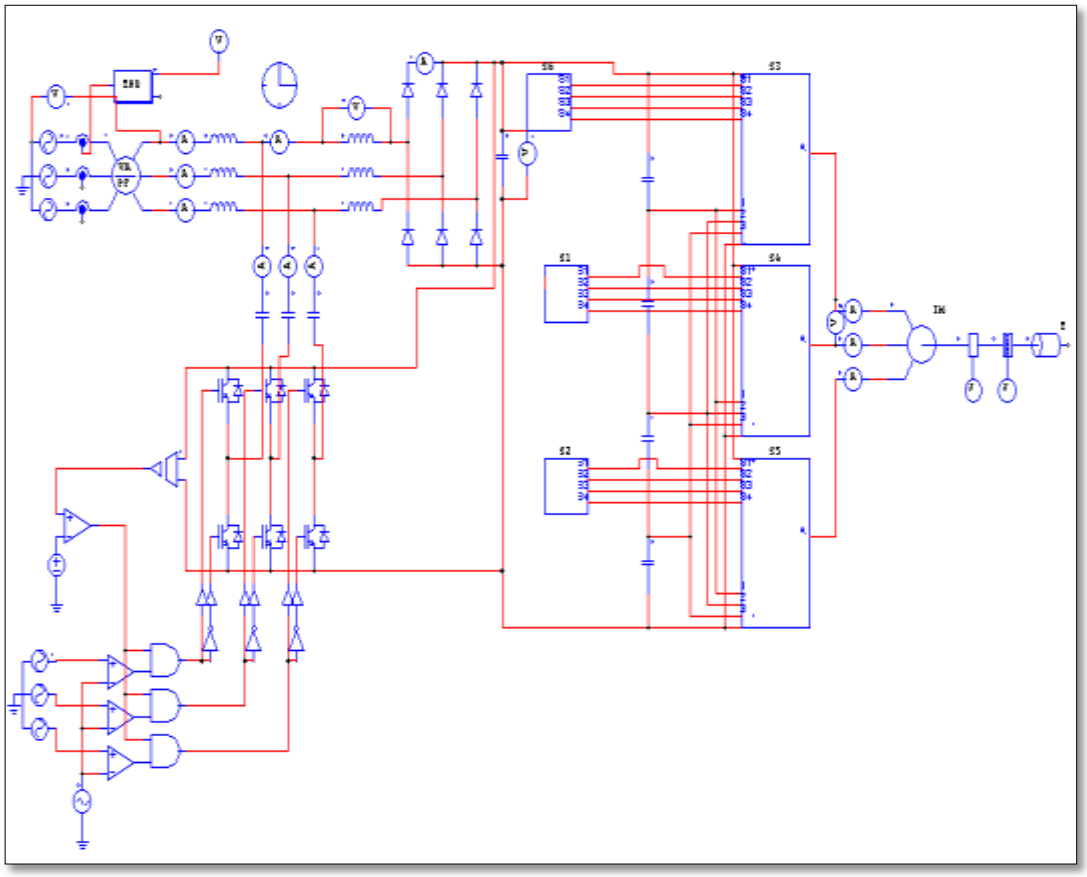

Figure 5.12 PSIM model of Nine level DCMLI fed induction motor with active current injection circuit

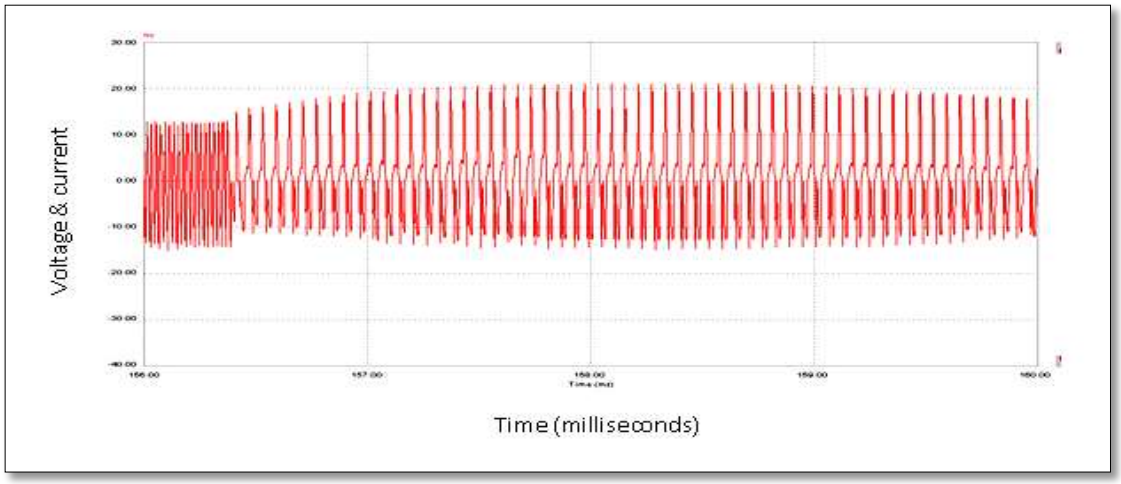

Figure 5.13 Injected current Ira:10V/div ,Time: 1msec/div

The Figure 5.13 shows the injected voltage, the current waveform to make the compensation on the distorted input current of diode rectifier. The active compensation network is added to inject the harmonic component in the diode rectifier input current. As a result, the harmonics present in the input current is reduced.

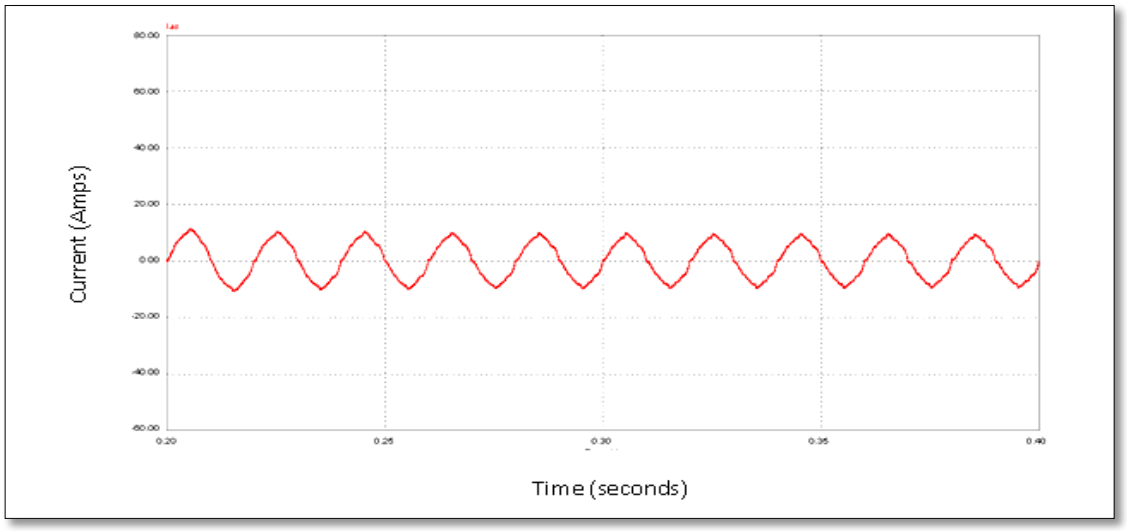

Figure 5.14 Source current with compensation 20A/div. Time: 0.05s/div

The Figure. 5.14 shows the per phase compensated input current of six-pulse diode rectifier. It is nearly sinusoidal when compared with passive compensation as shown in a Figure. 4.6

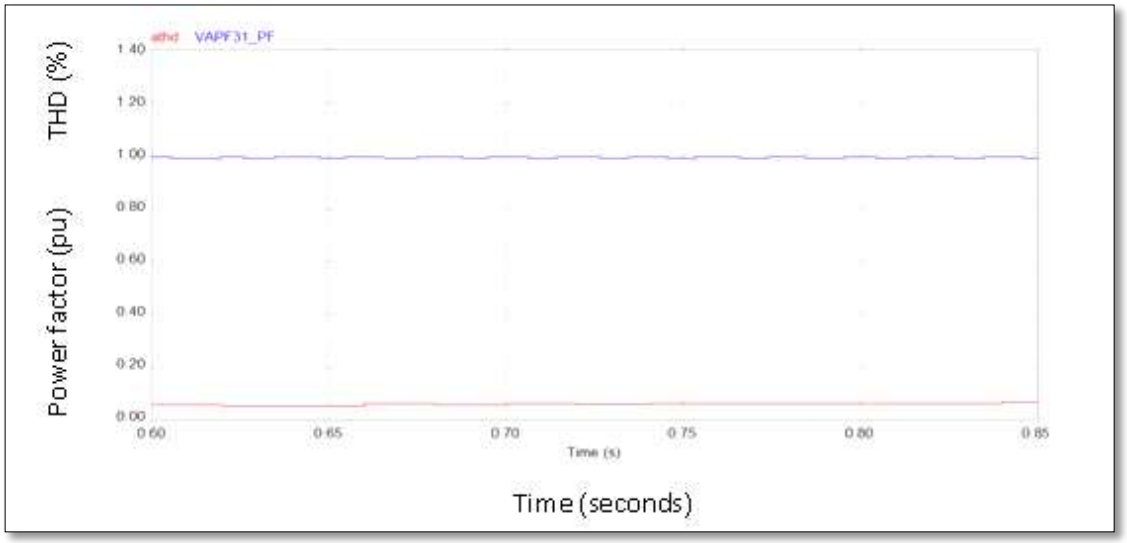

Figure 5.15 THD and PF; a thd (THD): 0.2pu/div. Time: 0.05s/div

The THD of supply current and PF obtained from simulation is shown in Figure 5.15.The total harmonic distortion of the compensated supply current is 5.76% and power factor is 0.99. This shows the improved performance when compared with existing results displayed in Figure. 4.7

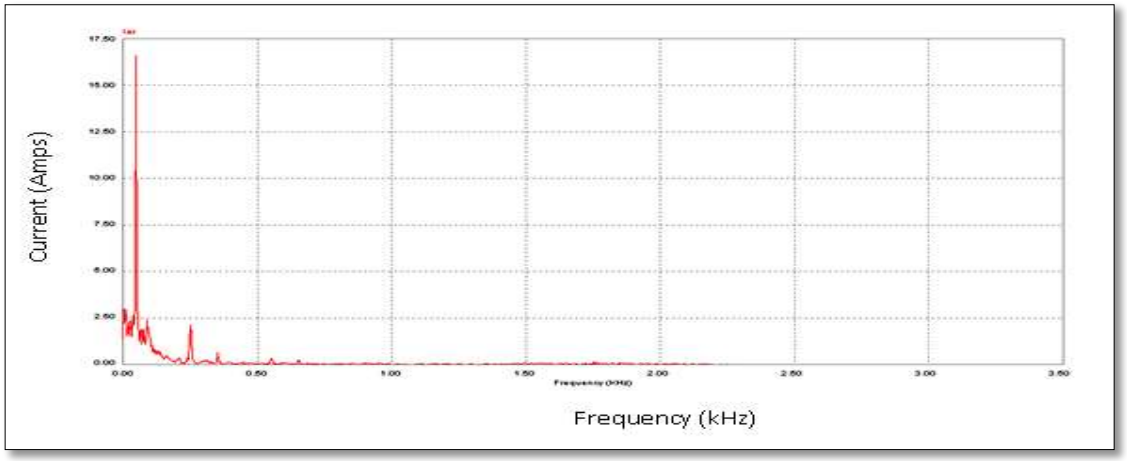

Figure 5.16. FFT spectrum 2.5A/div. Frequency: 0.5kHz/div

The Figure. 5.16 shows The FFT spectrum of the supply current is obtained from simulation. It explains the order of harmonics. Waveform clearly shows the absence of harmonic current.

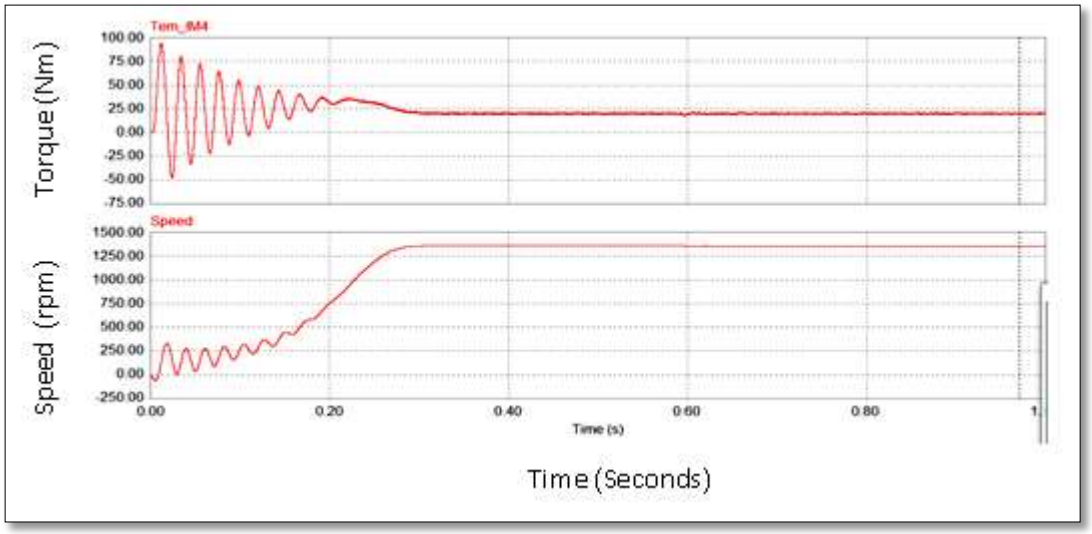

Figure.5.17. Torque and Speed at full load (Simulation)

Tem_IM4(Torque): 25Nm/div. Speed: 250rpm/div

Figure.5.17 shows the mechanical characteristics of speed and torque of

induction motor obtained from simulation. The inverter fed induction motor has smooth speed – torque characteristics. The speed of an induction motor is around 1350 rpm and 20 Nm torque is developed on the motor. The torque pulsation is almost zero. The settling time of the motor drive is about 0.3 Sec.

5.5 Experimental Results

There are several steps involved in implementing the hardware. Any power electronic system is divided into two of which one is the power unit and the other is the control unit. The complete block diagram is shown in figure 5.18. The control unit assembled with the pulse generation circuit, driver circuit and isolation circuit. The power unit constructed with power processing unit and input supply unit. To confirm the performance of the simulated system, the nine-level DCMI fed induction motor drive with active current injection is implemented with IGBTs as switching elements and is examined with the three phase 440 Volt squirrel cage induction motor coupled loading arrangements. In modern electric drives, high performance control is needed, which can be easily attained using advanced digital processors.

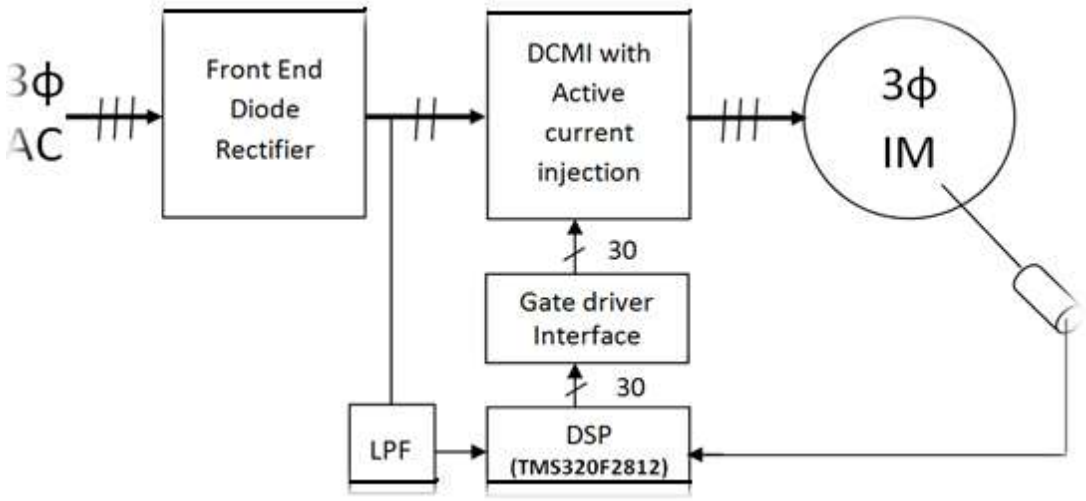

Figure 5.18. Complete block diagram of nine levels DCMLI with active injection network

The following values of components are selected for the experimental prototype and technical parameters of the AC motor is listed in Table 5.1

An analysis of the ac-dc-ac converter is carried out detailed in detail and based on the design, an experimental prototype of 2.5kW and output voltage of 540V is fabricated. For HF inverter IGBT module IRGB4059D is used. The Front-end rectifier is built with RHRP 30120 diodes. A digital signal processor (TMS320F 2812) is utilized to generate required gate pulses. The high-performance bipolar gate driver is built by using high-speed MOSFETs (IRF 510 and IRF 9510). This has assured better performance by avoiding false triggering of the IGBTs during their off state. The variable frequency control with fixed duty cycle is utilized to control the output voltage under different load conditions.

Table 5.1 Technical parameters of the AC motor

L_S = 0.5mH, C_a = 1F, L_a = 290H, C_o = 50F

Parameters	Values
Rated Power	2.5Kw
Rated Voltage	415V
Rated Current	6A
Rated Frequency	50Hz
Rated Speed	1400RPM
R_s, L_s	3.69Ω, 0.26H
Duty Cycle	S1
No. of Poles	4
Motor Type	Induction Motor
Connection	Star
No. of phases	Three Phase

5.5.1 Experimental setup

In order to perform experimental work, various components such as Three phase rectifier module, Hall effect current sensor module, Three phase Nine level inverter, Three phase 3 HP induction motor and DSO are arranged to get results. The experimental arrangement is shown Figure 5.19.

Figure 5.19. Experimental setup

A digital storage oscilloscope is an oscilloscope which stores and analyses the signal digitally. To validate the theoretical results, a low power, three-phase, nine levels MLI prototype is constructed. The inverter uses IRGB4059D (600V,8A) MOSFET as the switching devices. The reconfigurable MOSFET switches shown in Figure 5.20 configured as the proposed Nine level diode clamped inverter with the current injection network. It uses IC PC817 in the interface circuit. The gate control signals are generated by a dedicated unit, which is implemented on DSP processor TMS320F2812. Furthermore, an Atmel 8-bit AVR RISC microcontroller (ATmega16 L) is considered to interface with the operator and provide the switching times for DSP.

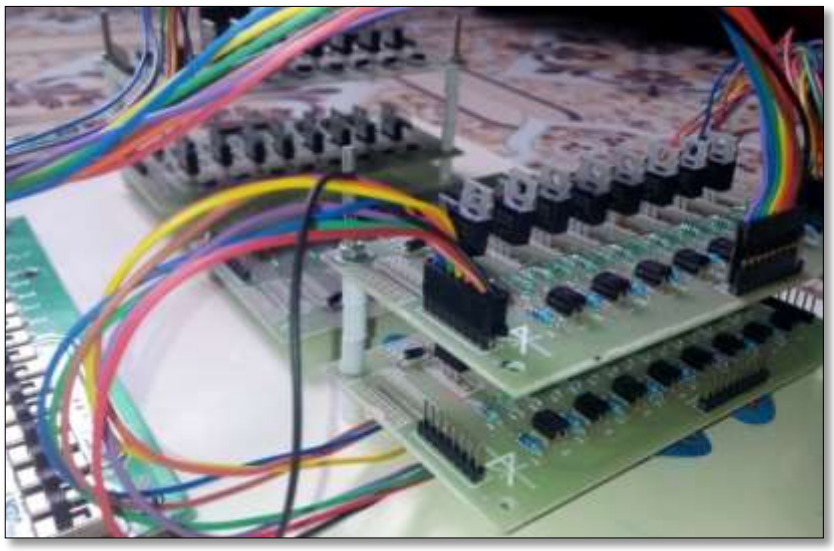

Figure 5.20. Reconfigurable MOSFET switches

5.5.2 Measurements

The experiment is carried out to monitor the input voltage and current of three phase diode rectifier and the output voltage and current of nine level MLI with and without current injection. Per phase readings of supply voltage and current are given below.

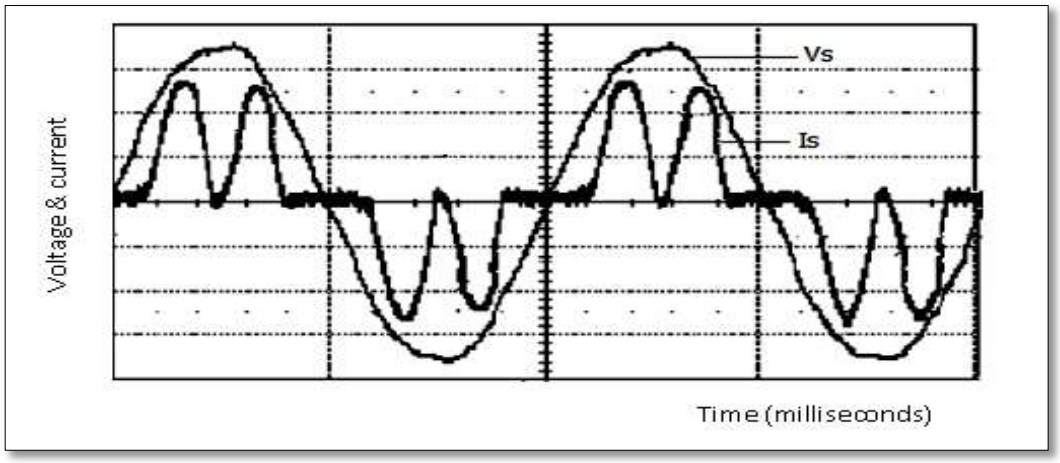

Figure. 5.21. Supply voltage (100V/div) and current (5A/div); x axis: 10ms/div

The phase A supply voltage and supply current obtained from experiment is shown in Figure. 5.21. It shows the distorted input current.

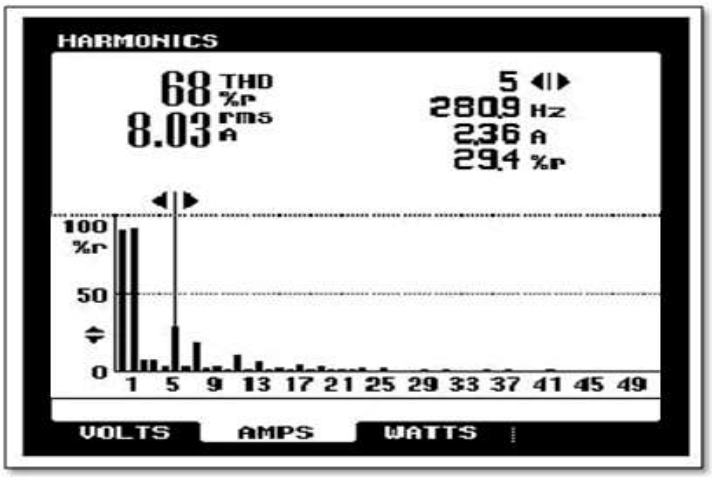

Figure 5.22. Harmonic spectrum of the input current, scale: Harmonic spectrum of the input current, scale: Y axis 2A/div: X axis: 100 Hz/div

The FFT spectrum of the supply current without compensation is obtained from experiment is shown in Figure. 5.22.

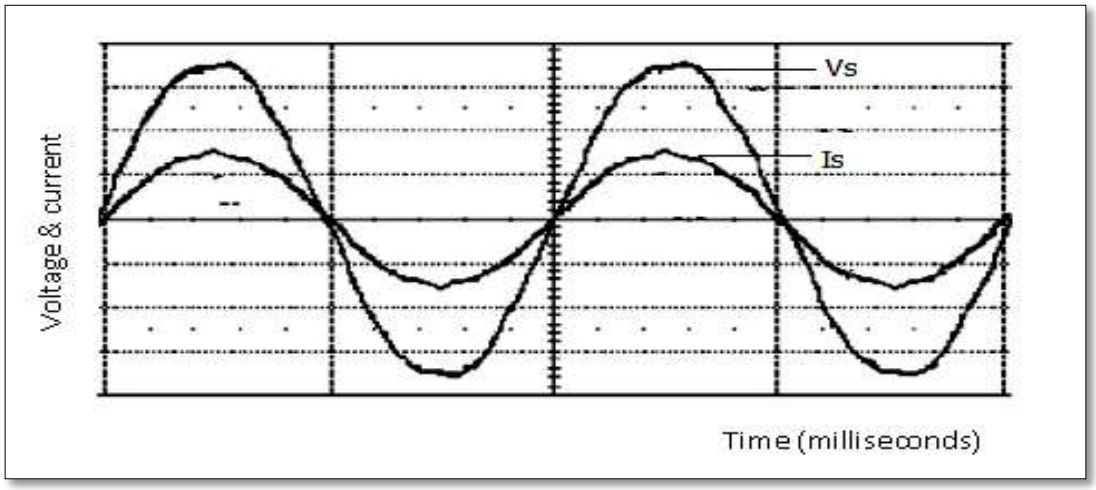

Figure 5.23Supply voltage (100V/div) and current (5A/div); x axis: 10ms/div

The phase A supply voltage and supply current obtained from experiment is shown in Figure. 5.23. It shows the compensated input current.

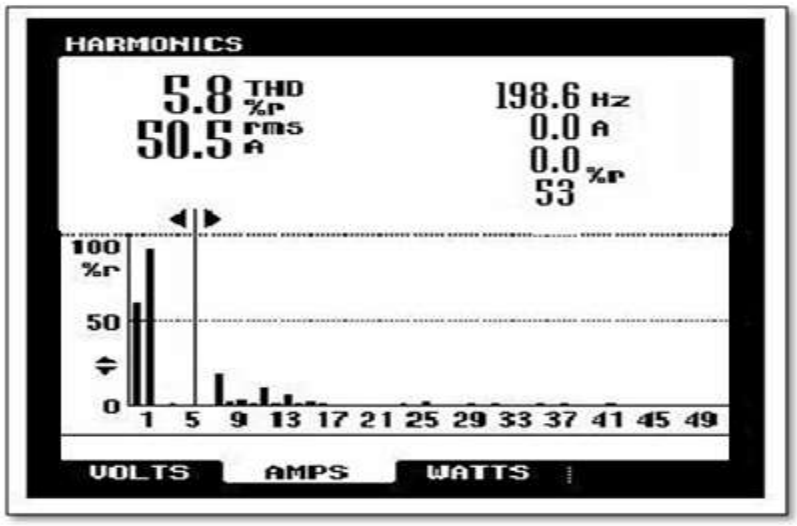

Figure 5.24 Harmonic spectrum of the input current, scale: Harmonic spectrum of the input current, scale: Y axis 2A/div: X axis: 100 Hz/div

The FFT spectrum of the supply current with compensation is obtained from experiment is shown in Figure. 5.24.

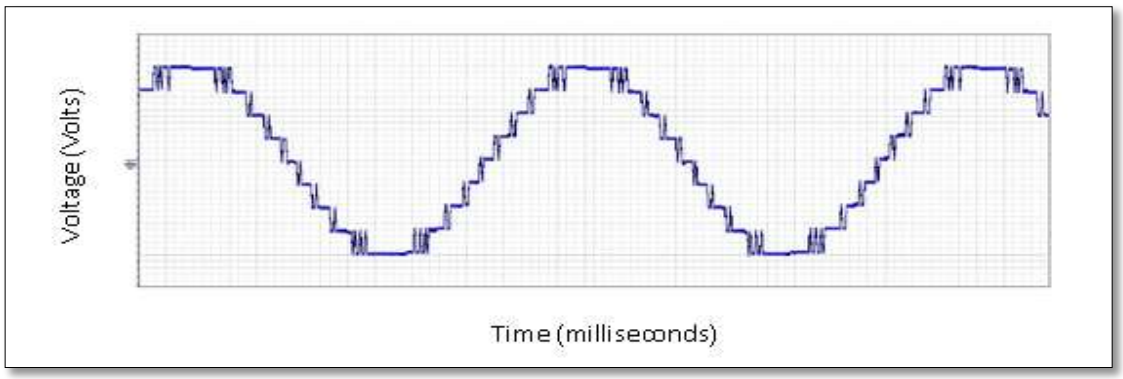

Figure 5.25. Multilevel Inverter per phase output voltage 100V/div; Time 5ms/div

The phase A output voltage of nine levels inverter is obtained from experiment is shown in Figure. 5.25.

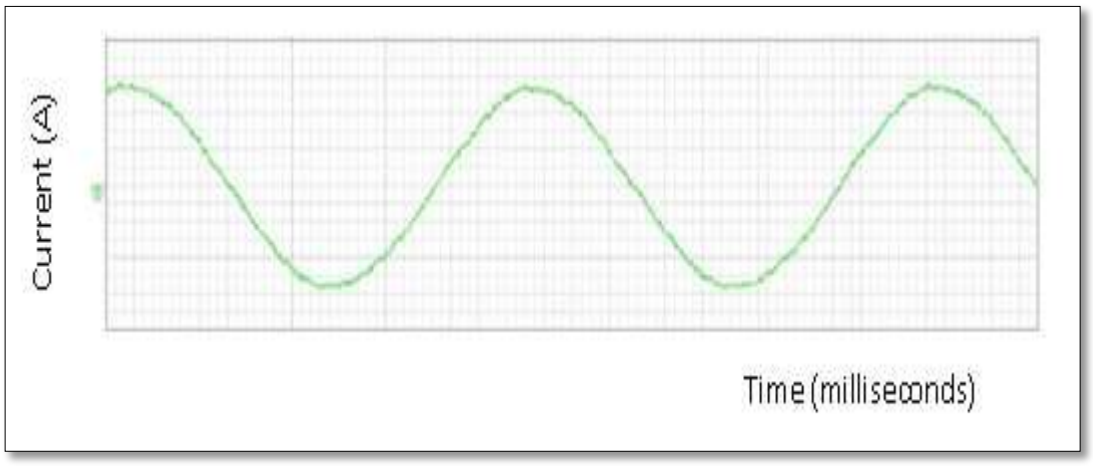

Figure 5.26. Multilevel Inverter per phase output current 5/div; Time 5ms/div

The phase A output current of multilevel inverter is obtained from experiment is shown in Figure. 5.26.

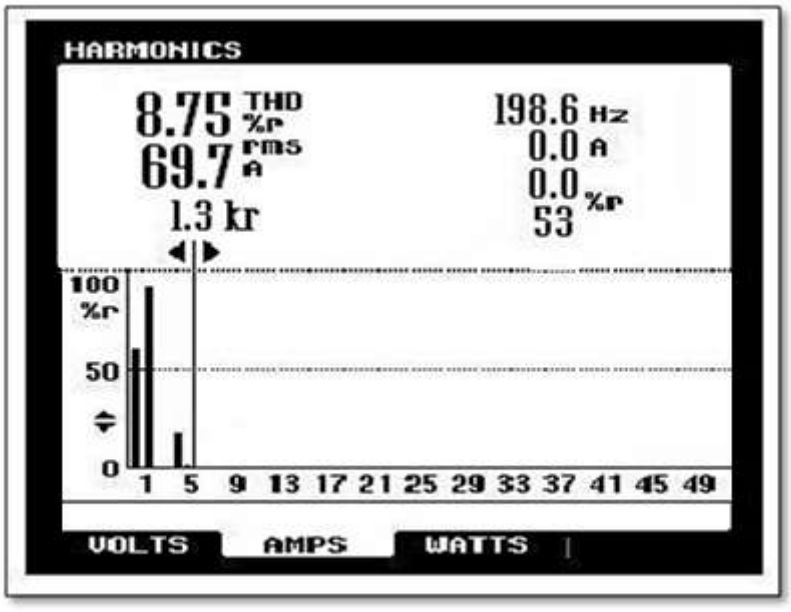

Figure 5.27Harmonic spectrum of the output current, scale: Harmonic spectrum of the output current, scale: Y axis 0.2pu/div: X axis: 200 Hz/div

The FFT spectrum of the output current is obtained from experiment is shown in Figure. 5.27. From the experiment, the observed parameters are tabulated in Table 5.2 and compared in graph.

Table 5.2 Performance comparison

Compensation	**Without**	**Passive Current Injection**			**Active Current Injection**		
Load Condition	**Full Load**	**Full Load**	**50% Load**	**25% Load**	**Full Load**	**50% Load**	**25% Load**
THD	68	7.72	10.2	12.7	5.76	8.1	9.9
PF	0.8	0.99	0.98	0.97	0.99	0.98	0.98

In Table 5.2, THD of supply current and input power factor are listed under different load conditions with & without current injection.

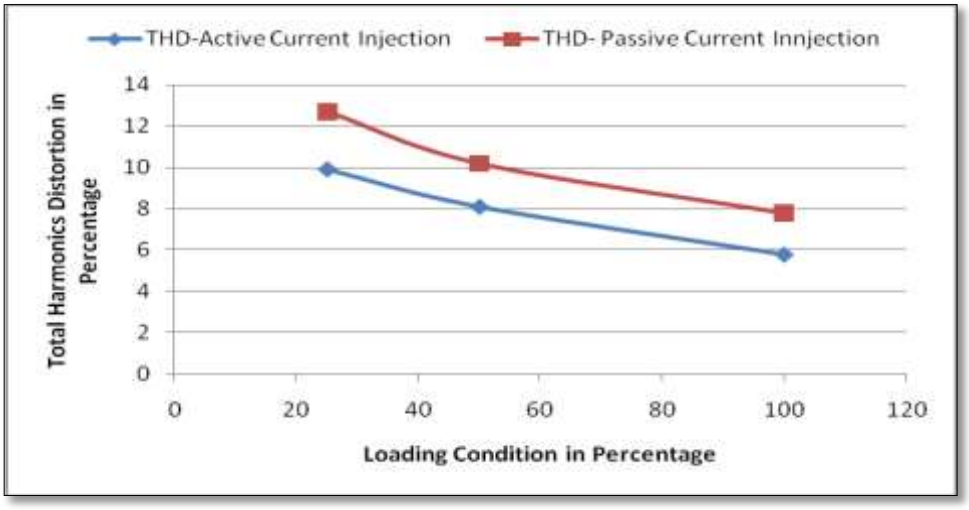

Figure 5.28. Percentage THD vs Load

The comparison between the percentage THD of Active current injection and passive current injection are plotted in Figure. 5.28. It shows that active current injection technique is better when compared with passive

current injection under different loading conditions.

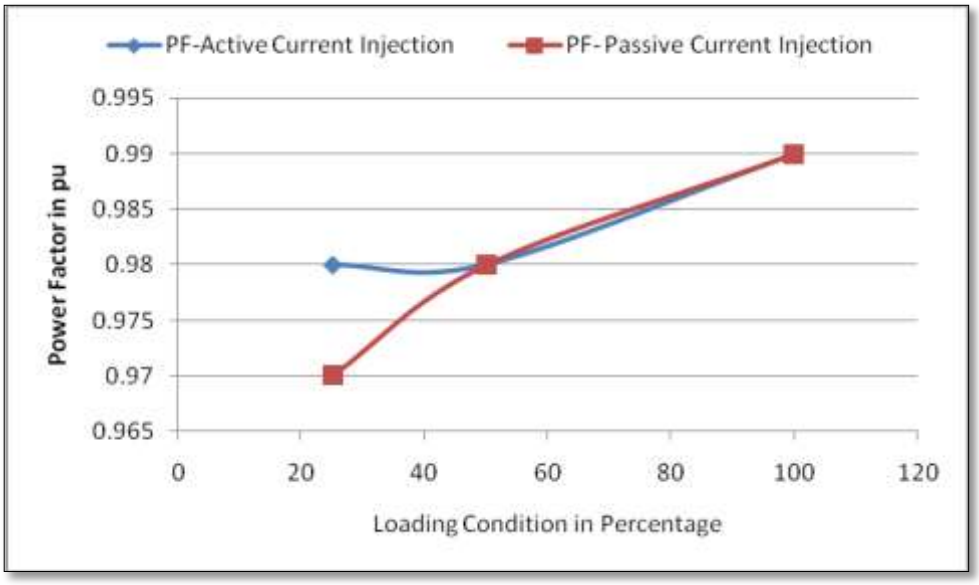

Figure 5.29. Power factor vs Load

The comparison between the input power factor of Active current injection and passive current injection are plotted in Figure. 5.29. It shows that active current injection technique is better when compared with passive current injection even at light load condition.

Table 5.3Comparison between Simulation and Experimental Results

Compensation technique	**Simulation Results THD (%)**	**Experimental Results THD (%)**
Passive Current Injection	7.72	7.8
Active Current Injection	5.76	5.8
Without compensation	85	68

The simulation results and experimental results are compared in Table 5.3.

5.6 Summary

A Nine level DCMLI with active current injection circuit is designed and its performance analyzed using PSIM simulation and experimentally verified. For the ease of understanding the operation of the active current injection network of the three phase AC-DC-AC converter, different modes of operation on the single-phase basis, are explained. Design equations of the active current injection network are derived which helps to design the vital components. The performance of the proposed system has been tested by experimentation. The results conformed to low THD and high-power-factor operation of the proposed system. The active current injection network of the three phase AC-DC-AC converter needs six active switches. But, it offers the following advantages. They are: less space requirement; soft-switching, reduction in filtering components size and EMI emissions, nearly Unity PF with regulated output voltage. The output voltage regulation at varying loads is obtained by controlling the switching frequency with fixed duty cycle in the proposed system. The converter can be utilized in medium to high power DC applications, variable DC drives, high current battery charger, etc.