Chapter 6

A CAD Tool for the Optimal Synthesis of Input Stage Differential Amplifier

6.1 Introduction

The rapid progress of design automation for digital integrated circuits (ICs) has enabled rapid synthesis of digital designs. Analog circuit design methodologies have not kept up with this pace. Although the circuit design software used by today's analog IC design engineers is more user friendly, and converges to solutions better than fifteen years ago, there has not been a parallel explosion of design capability for analog circuit designers. Today's analog circuit designers often use a combination of hand analysis and circuit simulation that was widely available in 1980. There has been some improvement in efficiency and capability since that time, due to the development of improved user interfaces for software tools, and new capabilities for behavioral, high level, and mixed signal simulation, but the task of circuit design is still reserved for experienced circuit designers using manual design and layout.

The general goal of Analog Computer Aided Design (ACAD) is to reduce the manual design and layout time required for circuit design. Improving analytical tools is a first step, and creating in-house cell libraries from previous designs is a low-tech way to speed circuit development through design re-use, but more aggressive techniques which result in design information reuse and automated design synthesis offer greater promise for reducing design time.

Analog circuit synthesis is a process in which design specifications such as amplification, bandwidth, *etc*. are used as inputs, to select appropriate circuit topologies, size devices and set the device biases. This process is not a one-to-one mapping, but usually is an under-constrained problem with many degrees of freedom. Also, since the process technology is just an input to the synthesis process, changing technology is no more complicated than changing the specifications. In either case the synthesis tool will create the best design for the input specifications.

In the present thesis, a CAD tool has been developed for the circuit synthesis of an optimal differential input stage operating in mid-frequency ranges, for the given maximum power budget, minimum differential voltage gain, minimum unity-gain bandwidth and a maximum input-referred noise. The circuit topology chosen is the same as shown in Fig. 4.1. The tool uses the methodology as described in the following section.

6.2 Implementation Methodology

From the given specifications in terms of maximum power budget, minimum differential voltage gain, minimum unity-gain bandwidth and maximum input-referred noise, we proceed as follows:

We know,

i) Unity-Gain Bandwidth of the differential input stage is given by

$$UGB = \frac{g_{mi}}{2\pi C_L}. \tag{6.1}$$

ii) Input-Referred Noise of the differential input stage at the gate of the input transistor is given by

$$IRN = \left[\frac{16}{3}\frac{kT}{g_{mi}}\left(1+\frac{g_{ml}}{g_{mi}}\right)\right]^{1/2} \tag{6.2}$$

ignoring flicker noise as thermal noise dominates the flicker noise in mid/moderate frequency ranges.

iii) Differential Voltage Gain of the differential input stage is written as

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} \tag{6.3}$$

Substituting the expressions for g_{mi}, g_{di} and g_{dl} from equations (3.4) and (3.9), we get

$$\begin{aligned} Ad &= \frac{\sqrt{k_n \left(\frac{W}{L}\right)_i I_{ref}}}{\frac{I_{ref}}{2}\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \\ &= \frac{2\sqrt{\frac{k_n}{L_i}}}{\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \frac{\sqrt{W_i}}{\sqrt{I_{ref}}} \end{aligned} \tag{6.4}$$

Let us choose the minimum permissible channel lengths for input and load transistors. Other parameters k_n, $\left(\frac{dx_d}{dV_{DS}}\right)_n$ and $\left(\frac{dx_d}{dV_{DS}}\right)_n$ being the technology parameters, Ad can be rewritten as

$$Ad = G \cdot \frac{\sqrt{W_i}}{\sqrt{I_{ref}}} \tag{6.5}$$

Where G is the technology constant given by

$$G = \frac{2\sqrt{\frac{k_n}{L_i}}}{\left[\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_p\right]} \tag{6.6}$$

where L_i and L_l are the minimum permissible channel lengths for the input and load devices.

After rearranging the equation, we can write

$$\sqrt{I_{ref}} = \frac{G}{Ad}\sqrt{W_i} \tag{6.7}$$

If we plot the graph between $\sqrt{I_{ref}}$ and $\sqrt{W_i}$ for different values of Ad it is as shown in Fig. 6.1. As the Ad increases, the slope of the line reduces. For a given value of Ad, there are infinite solutions possible in the $\sqrt{I_{ref}}$ and $\sqrt{W_i}$ space. For a the given maximum power budget, the maximum value of I_{ref} hence $\sqrt{I_{ref}}$ gets frozen which decides the minimum value of $\sqrt{W_i}$ from the constant Ad line (point A on Fig. 6.1).

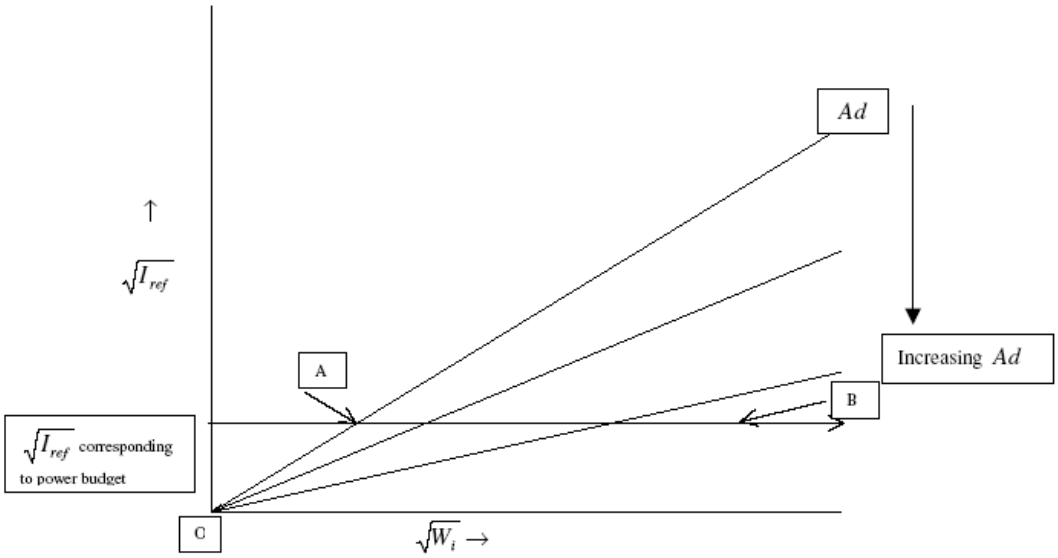


Figure 6.1 Variation of $\sqrt{I_{ref}}$ vs. $\sqrt{W_i}$ with Ad (differential dc voltage gain) as parameter.

iv) From these values of $\sqrt{I_{ref}}$ and $\sqrt{W_i}$, we can calculate a value of g_{mi}, as it is given by

$$g_{mi} = \sqrt{2\frac{k_n}{L_i}}\sqrt{W_i}\sqrt{I_{ref}}\,. \tag{6.8}$$

v) Find the minimum requisite g_{mi} to meet the UGB requirement from equation (6.1) under (i) above. If this value of g_{mi} is larger than the above calculated g_{mi}, then use this new g_{mi} as the minimum requisite g_{mi} of the circuit.

vi) To meet this new g_{mi}, the only parameter that can be altered is the width, W_i of the input transistor. To find the new W_i move on line AB (the constant power line chosen by power constraint) in Fig. 6.1 towards right hand side (lines for higher gain), which meets this g_{mi}.

vii) In order to find the required g_{mi} to meet the IRN requirements, manipulate the equation (6.2) given in (ii) above as under

$$\begin{aligned} g_{mi} &= \frac{-(-16kT) \pm \sqrt{(-16kT)^2 - 4 \times 3IRN^2(-16kTg_{ml})}}{2 \times 3IRN^2} \\ &= \frac{16kT \pm \sqrt{(16kT)^2 + 192IRN^2 kTg_{ml}}}{6IRN^2}. \end{aligned} \tag{6.9}$$

In this expression –ve sign will give a –ve g_{mi}, which is not a real solution and hence we take the solution with +ve sign. Secondly, g_{mi} is dependent on g_{ml}, which is further dependent on $\left(\frac{W}{L}\right)_l$. As g_{ml} increases g_{mi} reduces, but this dependance in very small, for large increase in L_l *i.e.* a large decrease in $\left(\frac{W}{L}\right)_l$ and hence a large reduction in g_{ml} results only in a small decrease in g_{mi}. Therefore, W_l and L_l are chosen to be the minimum permissible under the technology. Using these values g_{ml} is calculated and hence the minimum desired g_{mi} to meet the noise requirements. If this required g_{mi} is larger than the previously fixed g_{mi}, then the new g_{mi} is used to further find an enhanced value of W_i by moving to the right (increasing gain region) on the constant power line chosen.

viii) This gives the final values of device sizes and biasing for the differential amplifier circuit.

6.3 Verification by Simulation

The above methodology was coded using C, in a tool which was used to synthesize 2400 designs with different combinations of power budget, differential voltage gain, unity-gain bandwidth and input referred noise parameters in the ranges given below:

Power budget	—	100 – 1000 μW
Differential Voltage gain	—	10 – 1000
Unity Gain Bandwidth	—	1 – 1000 MHz
Input Referred Noise	—	1 – 20 nV/rtHz

The synthesized netlists of all the 2400 designs were simulated to compare their performance with the anticipated values of input-referred noise, differential dc voltage gain and unity-gain bandwidth.

6.3.1 Variation in Input-Referred Noise

The desired value of input-referred noise is plotted against the simulated value of input-referred noise for a fixed value of differential dc gain, Ad = 10 and UGB = 1 MHz as shown in Fig. 6.2. In absence of the error or in other words if simulated value perfectly matched with the desired value, then the graph should be a straight line with 45° inclination *i.e.* with slope as unity. But, the observed graphs do not show this behaviour in regions of low desired IRN. A closer look at the lines close to x-axis can be taken in Fig. 6.3.

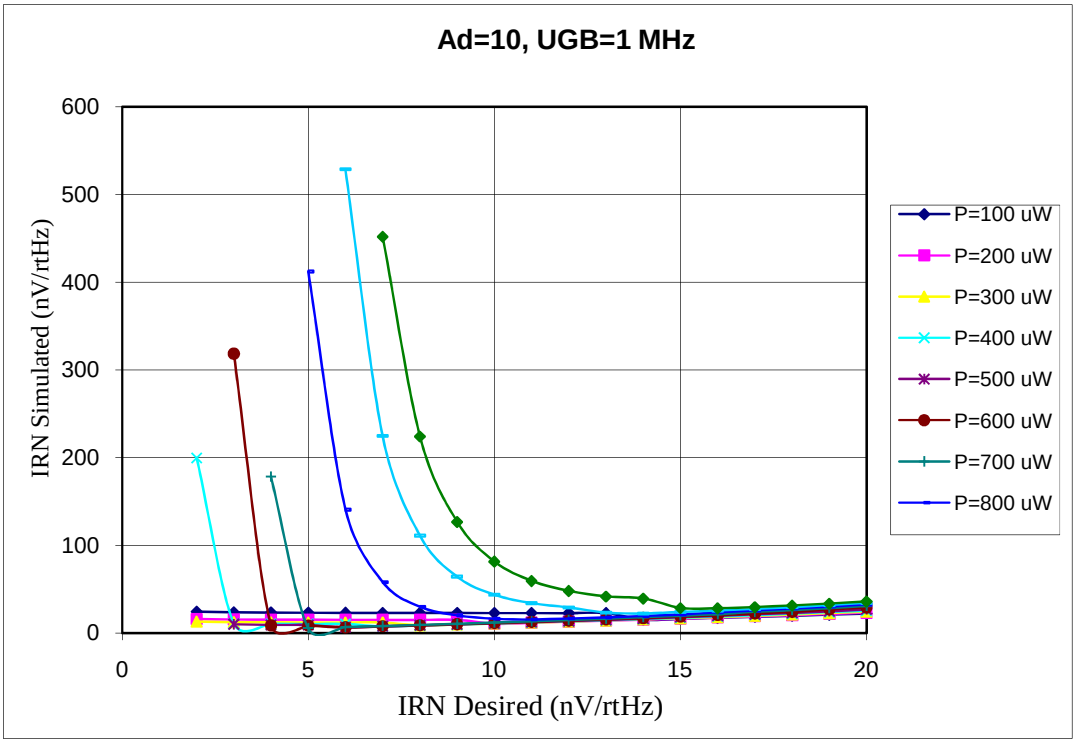


Figure 6.2 Variation in desired and simulated values of input referred noise at Ad=10 and UGB= 1 MHz.

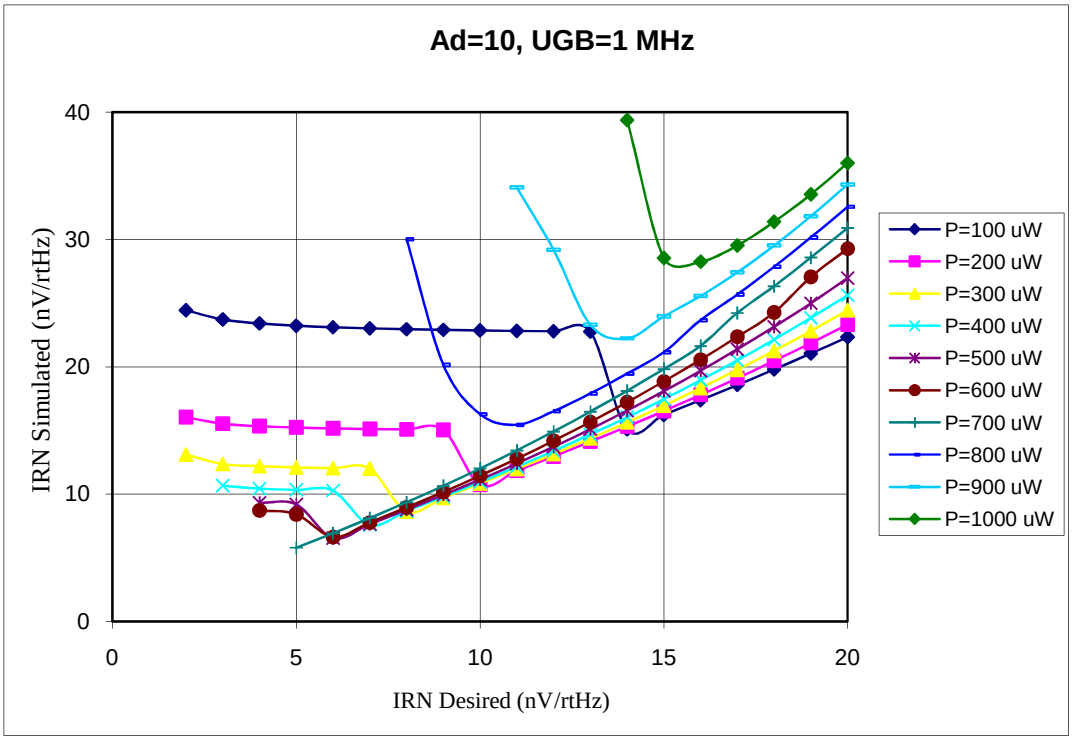


Figure 6.3 Close-up of lower portion of Fig. 6.2.

From the graph it is observed that the lines are straight upto a certain value of desired IRN below which the simulations predicted IRN increases sharply. This is because in these regions the input transistors leave the saturation region and go into the cutoff region. The slope is somewhat larger than unity, which implies that the simulated value of noise is slightly higher than the desired value and also changes with the power applied. In the case shown at desired value of 20 nV/rtHz, the simulated value is 22.3 nV/rtHz at 100 μW and it goes upto 36 nV/rtHz at 1000 μW. The reason for this variation with power is due to approximation of the model used, which has been explained in more detail in section 6.4. Every curve in the graph has a minima indicating that at this power, noise cannot be reduced beyond this point in the given technology. The minimum input referred noise achieved is 5.79 nV/rtHz at 700 μW.

Fig. 6.4 shows the desired value of input-referred noise plotted against the simulated value of input-referred noise for another combination of fixed values of differential dc gain, Ad = 10 and UGB = 100 MHz. It has been observed that with the demand of higher unity-gain bandwidth up to 100 MHz, the trend and values of simulated input-referred noise do not change.

However, it has been observed as shown in Fig. 6.5 that if an order of magnitude higher differential dc voltage gain is demanded, then the simulated input-referred noise patterns change significantly. The simulated input-referred noise is almost constant at a much lower value *e.g.* just 7.9 nV/rtHz at desired value of 8 to 20 nV/rtHz at the power of 700 μW and then further reduces up to 5.78 nV/rtHz at the desired value of 5.0 nV/rtHz and then increases sharply as shown in Fig. 6.6. It is also observed that at this high gain, if power larger than 700 μW is applied, then the noise increases to a much higher value for the reason that the input transistors leave the saturation region and move into the linear region of operation.

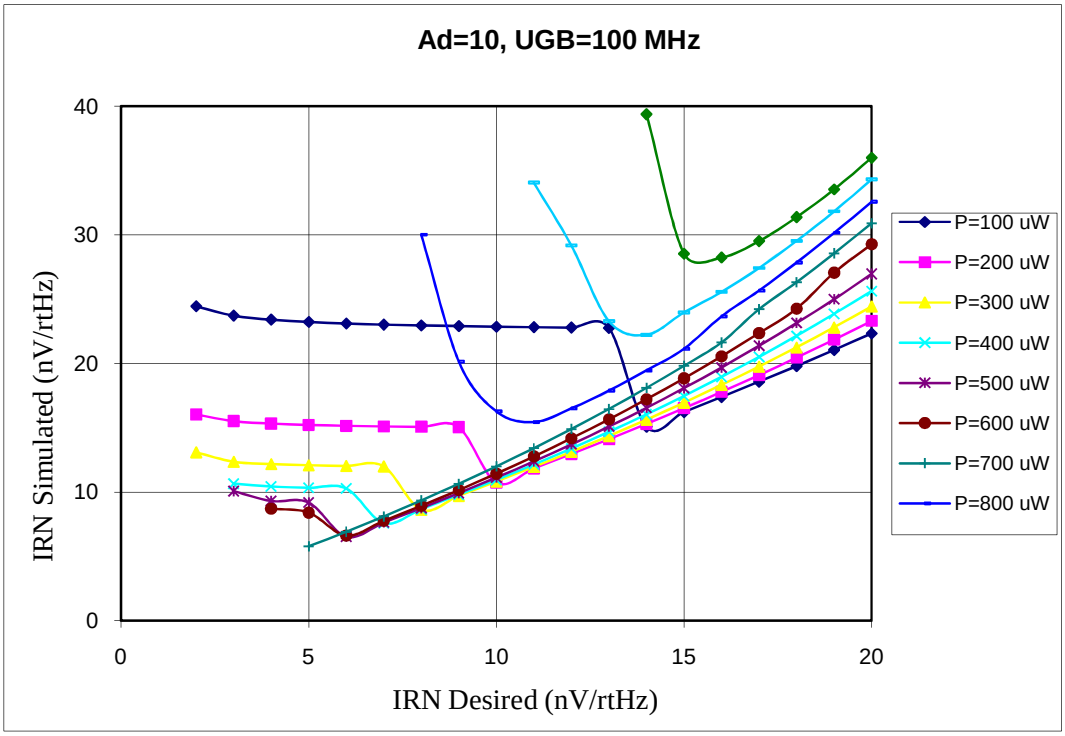


Figure 6.4 Variation in desired and simulated values of input referred noise at Ad=10 and UGB= 100 MHz.

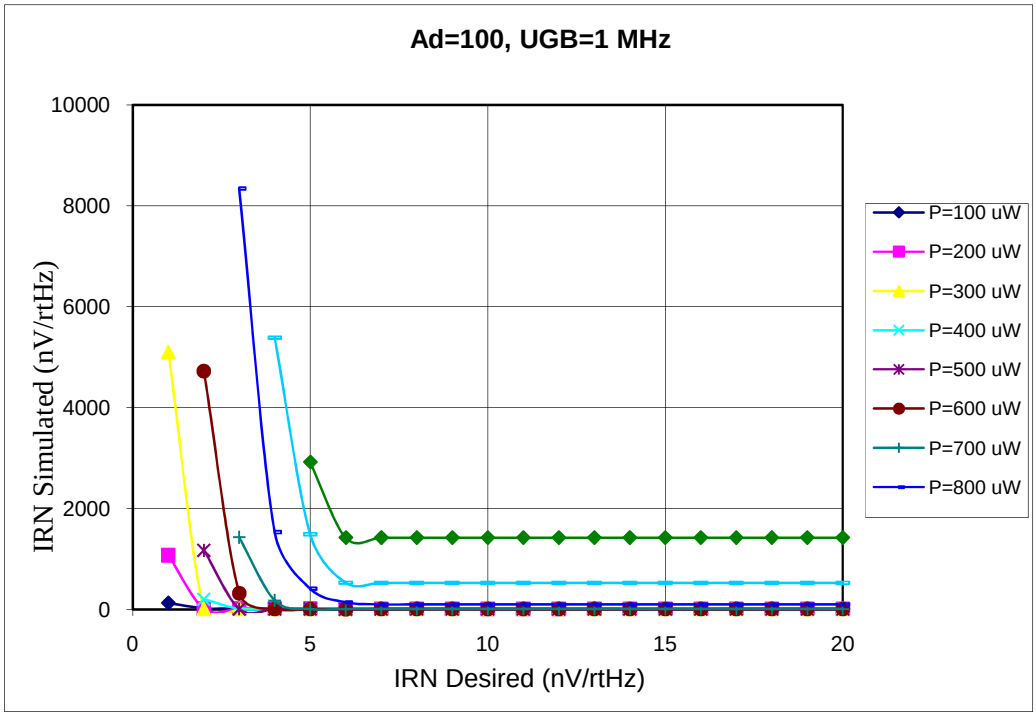


Figure 6.5 Variation in desired and simulated values of input referred noise at Ad=100 and UGB= 1 MHz.

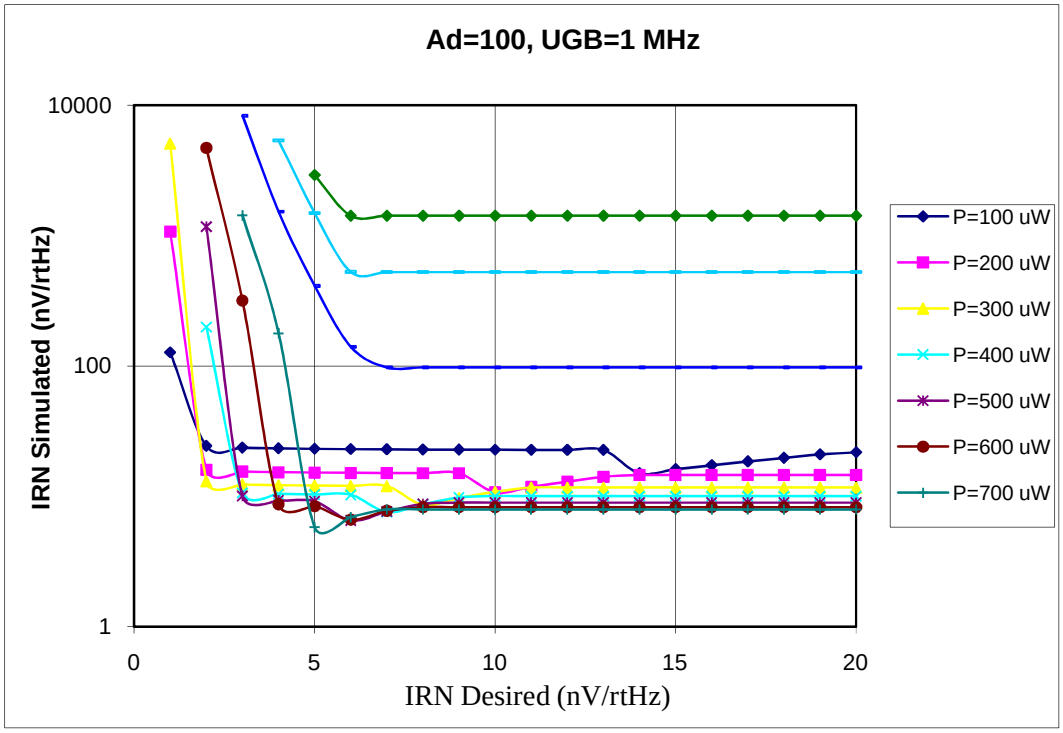


Figure 6.6 A close-up lower region of graph in Fig. 6.5.

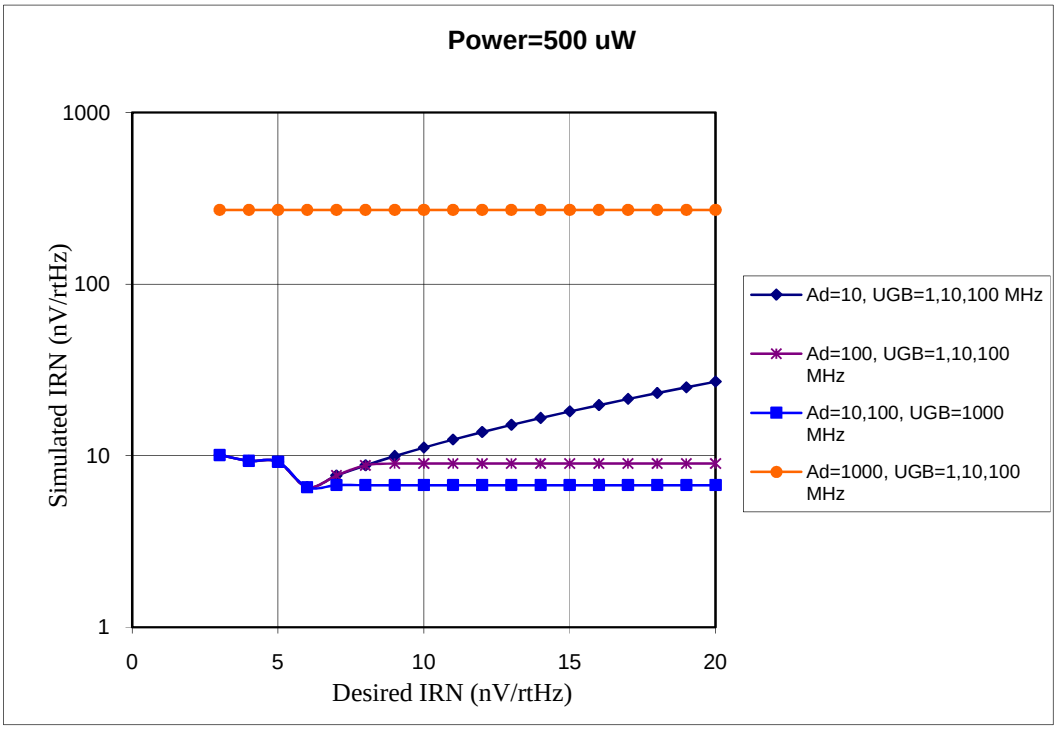


Figure 6.7 Variation in desired and simulated values of input referred noise with different combinations of Ad and UGB at a constant power of 500 μW.

Fig. 6.7 shows the variations between desired value of the input-referred noise and the simulated value of input-referred noise, for more combinations of differential dc voltage gain and the unity-gain bandwidths at the fixed power of 500 μW.

6.3.2 Area Power Trade-Off

An important trade-off between power and area always crops up in design. In order to meet other design objectives can we reduce area at the cost of power in area-constraint designs or can we reduce power at the cost of area in power conscious designs? The answer is yes. Fig. 6.8 analytically plots the area required for various values of input-referred noise, at different levels of applied power. From the graph it is clearly seen that at a given value of input-referred noise, the area required increases as the power applied reduces and vice-a-versa. The simulated equivalent graph is shown in Fig. 6.9, which validates the above observation over a substantial range. However, it deviates at the lower values of noise for powers below and up to 700 μW, because input transistors are in cutoff region and at high powers these transistors move into the linear region of operation. In either case the noise increases substantially as the current models used are valid only in the saturation region of operation.

6.4 Boundary Conditions

In this section, it has been attempted to bring out the boundary conditions in which the tool operates and gives satisfactory results. Beyond the boundary conditions, the tool may not give reasonable results. The boundary conditions have been found in terms of the minimum input referred noise, maximum differential dc voltage and maximum unity-gain bandwidth that can be achieved; and the power range that gives the best performance.

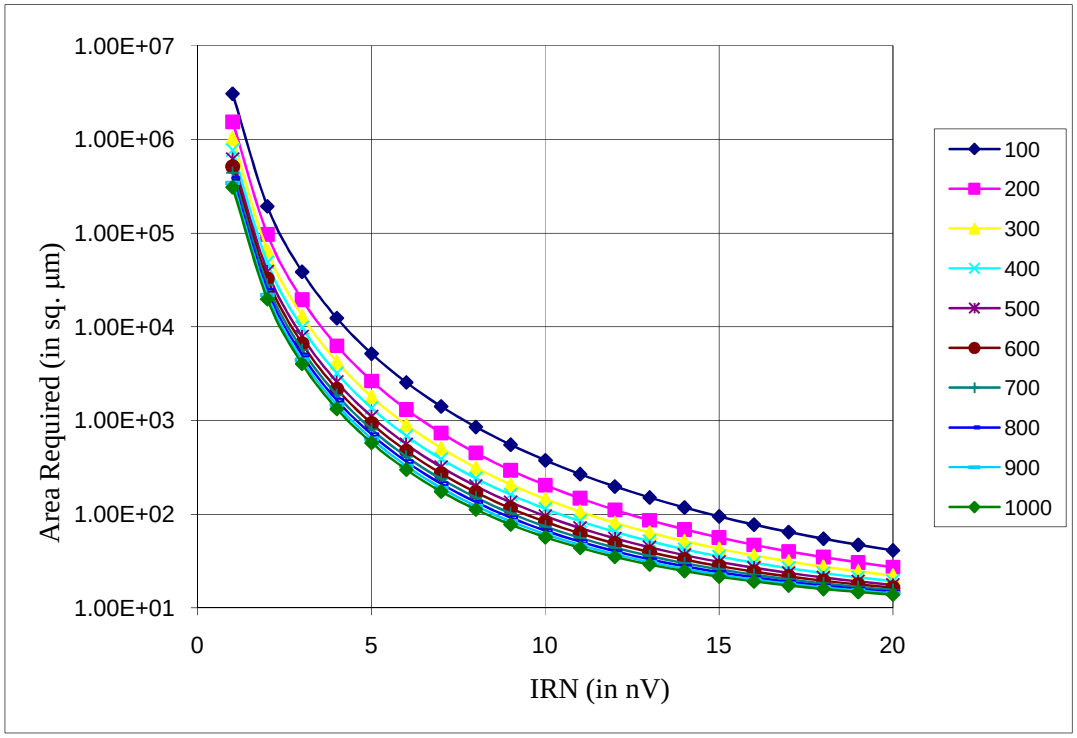


Figure 6.8 Analytical Area-Power trade off with varying input referred noise.

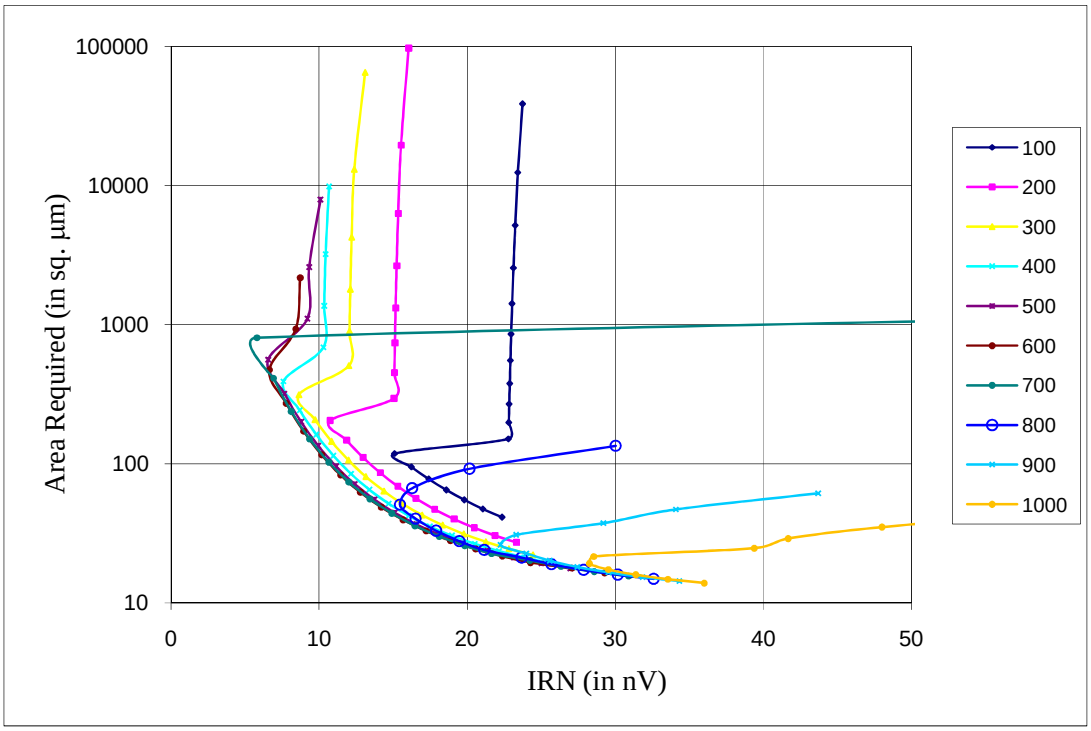


Figure 6.9 Simulated Area-Power trade off with varying input referred noise.

6.4.1 Power Range

Figure 6.10 plots the minimum achieved input referred noise as a function of power applied to the circuit. It is evident from the plot that to achieve a low noise circuit increasing or decreasing power beyond a limit is not going to help. However, the minimum value of thermal noise for the circuit is observed at 700 μW, the optimum value of power in this case appears to be in the range of 300 μW – 700 μW.

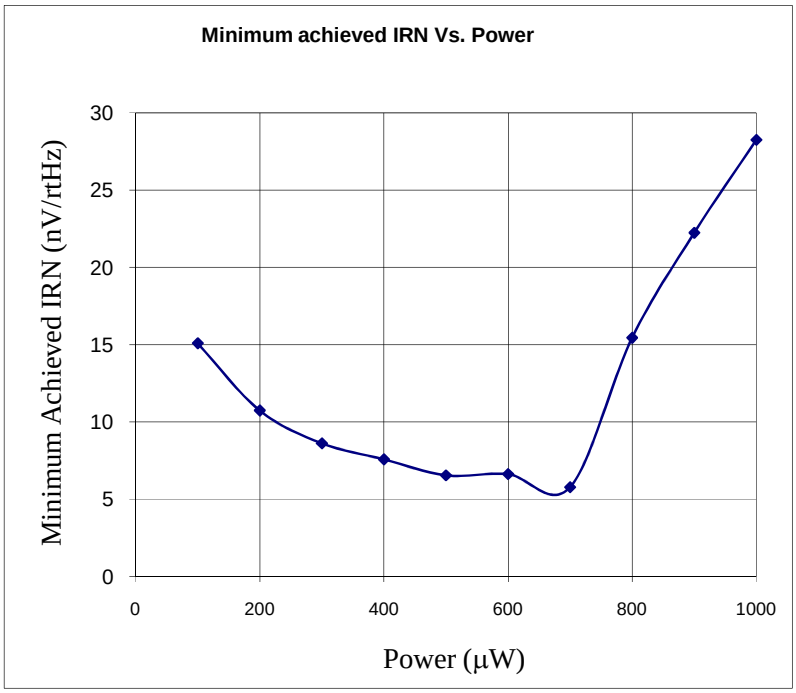


Figure 6.10 Minimum achieved IRN as a function of Power.

6.4.2 Limit on Noise Reduction, Gain and Bandwidth Enhancement

Clearly, from the previous discussions, there is a limit on each parameter, *i.e.* the best values that can be achieved for a technology. In the current technology based on the simulations performed on the designs, which were synthesized using this tool, minimum value of input referred noise that could be achieved is 5.3 nV/rtHz at 700 μW as seen in Fig. 6.10. The maximum value of differential dc voltage

gain achieved is 60.4 at 100 μW (refer Fig. 6.11) and the maximum value of unity gain bandwidth is 261.2 MHz at 700 μW (see Fig. 6.12).

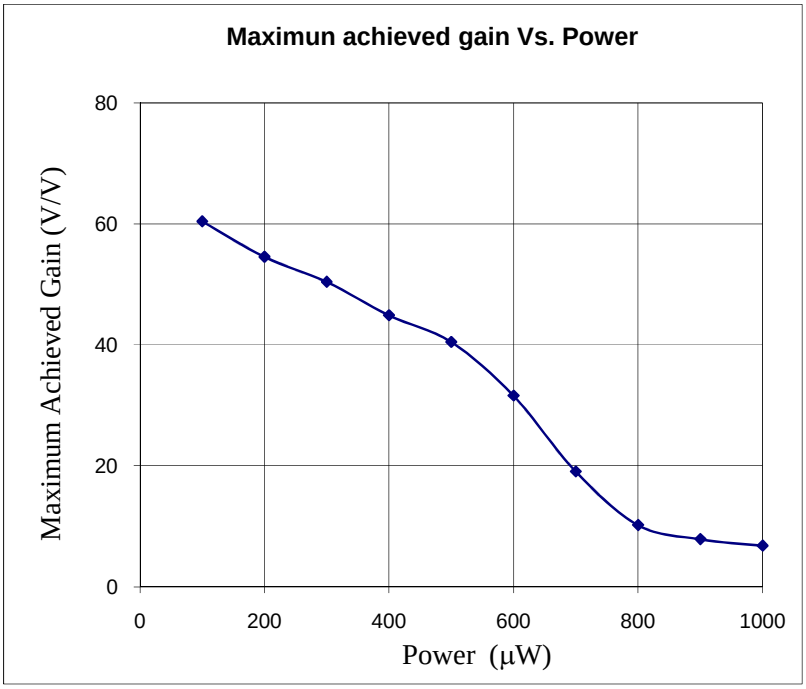


Figure 6.11 Maximum achieved differential dc voltage gain as a function of power.

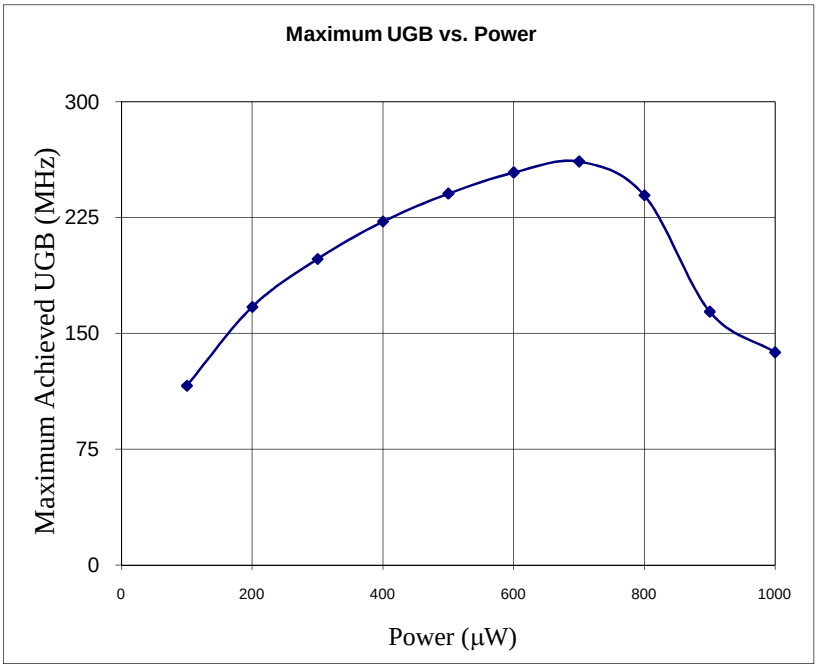


Fig. 6.12. Maximum achieved unity-gain bandwidth as a function of power.

6.5 Some Practical Implications

Whether a desired combination of differential gain, unity gain bandwidth and input referred noise is possible to achieve at all in a given technology is a question that needs to be engaged into. Limits and limiting relationships need to be explored in terms of the technology parameters, which govern differential gain, unity gain bandwidth and input referred noise.

This section is devoted to the exploration of limits and limiting relationships on differential dc voltage gain, Ad and unity gain bandwidth, UGB of an unloaded differential amplifier.

Since, the differential dc voltage gain, Ad and unity-gain bandwidth, UGB of a differential amplifier with the current mirror load (Fig. 4.1) are given by equations (4.14) and (4.15) reproduced below

$$UGB = \frac{g_{mi}}{2\pi \cdot C_L} = \frac{1}{2\pi \cdot C_L}\sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \tag{6.10}$$

$$Ad = \frac{g_{mi}}{g_{di} + g_{dl}} = 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \tag{6.11}$$

All symbols have their usual meaning as mentioned in chapter 4.

The product of the differential dc voltage gain and unity-gain bandwidth can be written as

$$\begin{aligned} Ad * UGB &= \frac{1}{2\pi \cdot C_L}\sqrt{\frac{k_n \cdot W_i \cdot I_o}{L_i}} \cdot 2 \cdot \sqrt{\frac{k_n}{I_o} \cdot \left(\frac{W_i}{L_i}\right)} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \\ &= \frac{k_n}{\pi \cdot C_L} \cdot \frac{W_i}{L_i} \cdot \left(\frac{1}{L_i}\left(\frac{dx_d}{dV_{DS}}\right)_n + \frac{1}{L_l}\left(\frac{dx_d}{dV_{DS}}\right)_n\right)^{-1} \end{aligned} \tag{6.12}$$

From section (3.3.3) substituting the values of $\left(\frac{dx_d}{dV_{DS}}\right)$ for n and p transistors in equation (6.12), it can also be written as

$$Ad * UGB = \frac{10k_n \cdot W_i}{\pi \cdot C_L} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \tag{6.13}$$

For an unloaded amplifier, the external capacitance is zero implying that the drain-to-bulk capacitances of the input and the load transistors form the capacitive load [Johns97], *i.e.*

$$C_L = C_{dbi} + C_{dbl} \tag{6.14}$$

where C_{dbi} and C_{dbl} are the drain-to-bulk capacitances of the input and load transistors respectively.

For a transistor the drain-to-bulk capacitance is given by

$$C_{db} = C'^{'}_{db} + C_{d-sw} \tag{6.15}$$

where C'_{db} is bottom plate capacitance of the drain junction and C_{d-sw} is the side wall capacitance of the drain junction.

Further,

$$C'_{db} = A_d \cdot C_{jd} \tag{6.16}$$

A_d is the area of the bottom plate of the junction, which is same as the drain area and C_{jd} is the junction capacitance per unit area for the one-sided step junction and is given by

$$C_{jd} = \frac{C_{j0}}{\sqrt{1 + \frac{V_{DB}}{\phi_0}}} \tag{6.17}$$

where C_{j0} is the zero-bias junction capacitance and is a process constant given by

$$C_{j0} = \sqrt{\frac{qK_s\varepsilon_0 N_D}{2\phi_0}} \tag{6.18}$$

and V_{DB} is the drain-to-bulk potential of the junction. All other symbols have their usual meanings.

The built-in potential, ϕ_0 is given by

$$\phi_0 = V_T \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right). \tag{6.19}$$

The sidewall capacitance of the drain region, C_{d-sw} is given by

$$C_{d-sw} = P_d \cdot C_{j-sw} \tag{6.20}$$

where P_d is the perimeter of the drain region excluding the portion/wall adjacent to the gate and

$$C_{j-sw} = \frac{C_{j\_sw0}}{\sqrt{1+\frac{V_{DB}}{\phi_0}}}. \tag{6.21}$$

Hence the drain-to-bulk capacitance of a transistor can be written as

$$C_{db} = A_d \cdot C_{jd} + P_d \cdot C_{j-sw} \tag{6.22}$$

For the input transistor (n-type) we rewrite it as

$$C_{dbi} = \left(W_i * L_{d,n}\right) \cdot C_{jd,n} + \left(W_i + 2L_{d,n}\right) \cdot C_{j-sw,n} \tag{6.23}$$

and for load transistor (p-type)

$$C_{dbl} = \left(W_l * L_{d,p}\right) \cdot C_{jd,p} + \left(W_l + 2L_{d,p}\right) \cdot C_{j-sw,p} \tag{6.24}$$

where $L_{d,n}$ and $L_{d,p}$ are the lengths of drain extensions beyond the gate for n-type and p-type transistors respectively.

In order to simplify the overall expression of the product $Ad*UGB$, we make the following assumptions:

i) Typically drain extends 4λ beyond the gate, therefore

$$L_{d,n} = L_{d,p} = 4\lambda \tag{6.25}$$

ii) Since the differential gain and unity-gain bandwidth are independent of width of the load transistor, W_l, it can be chosen to be minimum *i.e.* 2λ. With this

$$C_{dbi} = (W_i * 4\lambda) \cdot C_{jd,n} + (W_i + 2 * 4\lambda) \cdot C_{j-sw,n} \tag{6.26}$$

$$C_{dbl} = (2\lambda * 4\lambda) \cdot C_{jd,p} + (2\lambda + 2 * 4\lambda) \cdot C_{j-sw,p} \tag{6.27}$$

iii) Further, if we approximate that $C_{jd,n} \sim C_{jd,p} = C_{jd}$ and $C_{j-sw,n} \sim C_{j-sw,p} = C_{j-sw}$, the total load capacitance is given by

$$C_L = C_{dbi} + C_{dbl} = (W_i + 2\lambda) \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \tag{6.28}$$

iv) For most analog applications, to increase the input transistor trans-conductance, $W_i >> 2\lambda$, which further reduces equation (6.28) to the approximation

$$C_L \approx W_i \cdot 4\lambda \cdot C_{jd} + (W_i + 18\lambda) \cdot C_{j-sw} \tag{6.29}$$

Eqn. (6.29) can also be written as

$$C_L = W_i \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right] \cdot \tag{6.30}$$

Substituting this as the load in equation (6.13) the upper bound on the product $Ad*UGB$ becomes

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + \left(1 + \frac{18\lambda}{W_i} \right) \cdot C_{j-sw} \right]} \cdot \left(1 + \frac{L_i}{2.L_l} \right)^{-1} \tag{6.31}$$

v) Further, for most analog applications $W_i >> 18\lambda$, then the above equation (6.31) further reduces to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \cdot \left(1 + \frac{L_i}{2.L_l}\right)^{-1} \tag{6.32}$$

vi) Also, typically $L_i << L_l$, which further reduces the above expression (6.32) to

$$Ad*UGB < \frac{10k_n}{\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \tag{6.33}$$

This is a pure technology constant. Therefore, we can say that the product $Ad*UGB$ is a technology constant.

Even if $L_i << L_l$ is not true, and $L_i = L_l$ as in our case, the equation (6.32) reduces to

$$Ad*UGB < \frac{20k_n}{3\pi \cdot \left[4\lambda \cdot C_{jd} + C_{j-sw}\right]} \tag{6.34}$$

which is also a technology constant.

Equation (6.31) with $L_i = L_l$, is plotted as a function of W_i for several technologies as shown in Fig. 6.13. Clearly $Ad*UGB$ becomes independent of W_i for wide transistors and is a constant for a technology. It implies that gain of the circuit in a technology can only be increased at the cost of unity-gain bandwidth or vice-a-versa. The value of $Ad*UGB$ at $W_i = 500\mu m$ in various technologies has been plotted in Fig. 6.14. It is evident that in most cases the value of $Ad*UGB$ increases with the scaling of technology.

The simulated values of $Ad*UGB$ for 1.2 μm CMOS technology have been plotted in Fig. 6.15. Here, it is observed that the $Ad*UGB$ product becomes a function of the power applied to the circuit although in the analytical model it is independent of the power. This is because of the approximate model used for

channel length modulation, λ. It is assumed to be constant but actually it varies with the current flowing through the transistor.

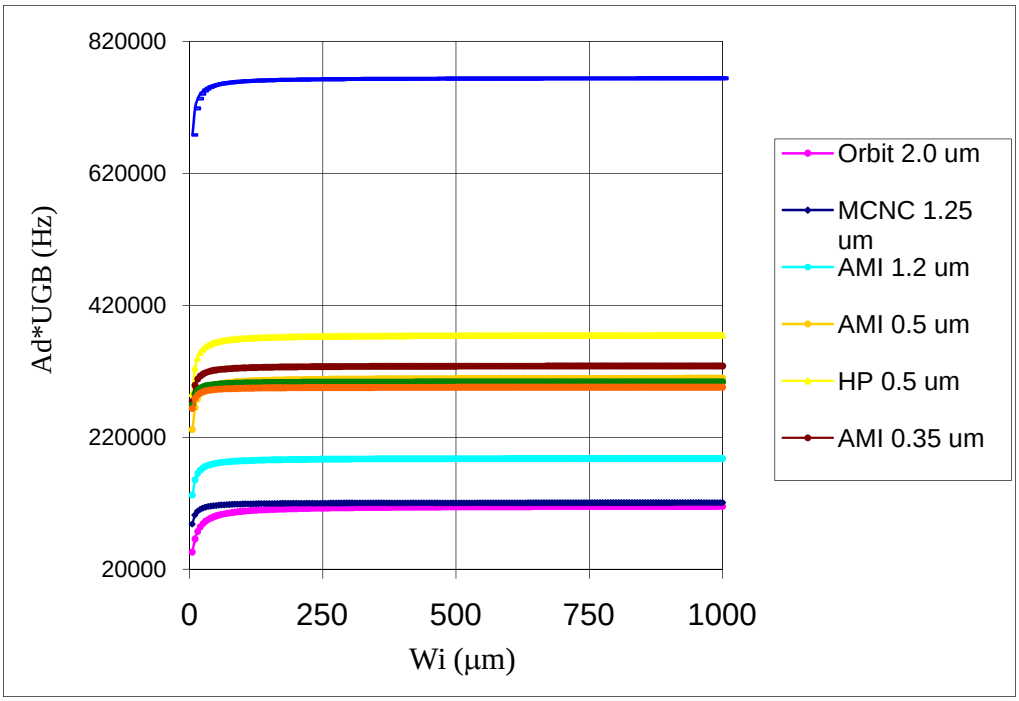


Figure 6.13 Analytical Ad*UGB product variation with technology.

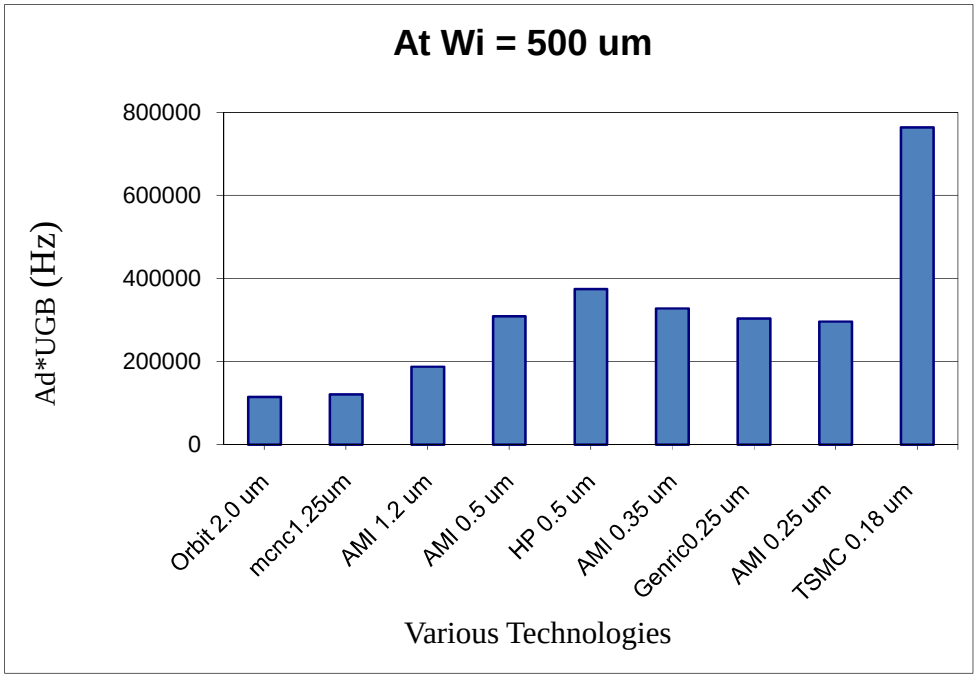


Figure 6.14 Ad*UGB product variation at $W_i = 500\mu m$ for various technologies.

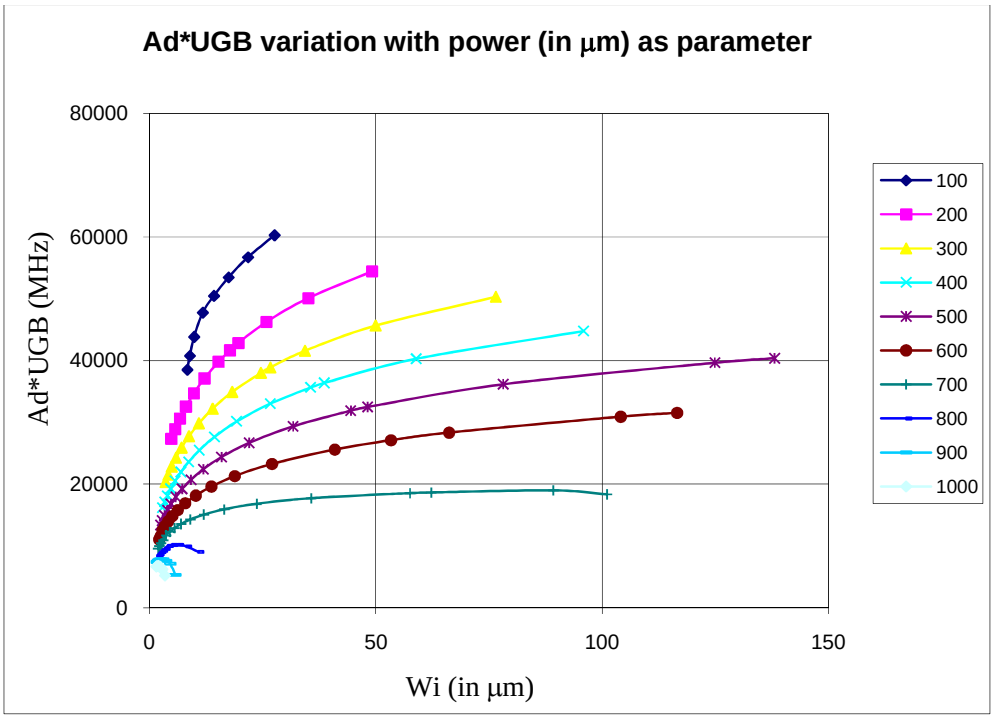


Figure 6.15 Simulated Ad*UGB product variation with power in MCNC 1.25 μm CMOS technology.

The above results (both analytical and simulated) were obtained with no external load connected to the output of the differential amplifier. Only the parasitic drain capacitance loads of the input and load transistors were considered. However, given that the unity gain bandwidth, UGB is inversely proportional to the load connected at the output of the differential amplifier, the limiting value of the gain unity-gain bandwidth product, $Ad*UGB$ for an amplifier loaded with external capacitor of value C_L can be worked out as

$$(Ad*UGB)_{loaded} = \frac{(Ad*UGB)*(C_{di}+C_{dl})}{(C_{di}+C_{dl}+C_L)} \tag{6.35}$$

$$= \frac{(Ad*UGB)}{1+\left(\frac{C_L}{C_{di}+C_{dl}}\right)} \tag{6.36}$$

$$= f_{load}*(Ad*UGB) \tag{6.37}$$

where f_{load} is a load dependent degradation factor defined by

$$f_{load} = \frac{1}{1 + \frac{C_L}{(C_{di} + C_{dl})}} \tag{6.38}$$

Equations (6.37) and (6.38) provides a rapid way of computing the loaded gain unity-gain bandwidth product, $Ad*UGB$ for any differential amplifier given its unloaded $Ad*UGB$ product. Fig. 6.16 shows how the $Ad*UGB$ product varies with the external load C_L.

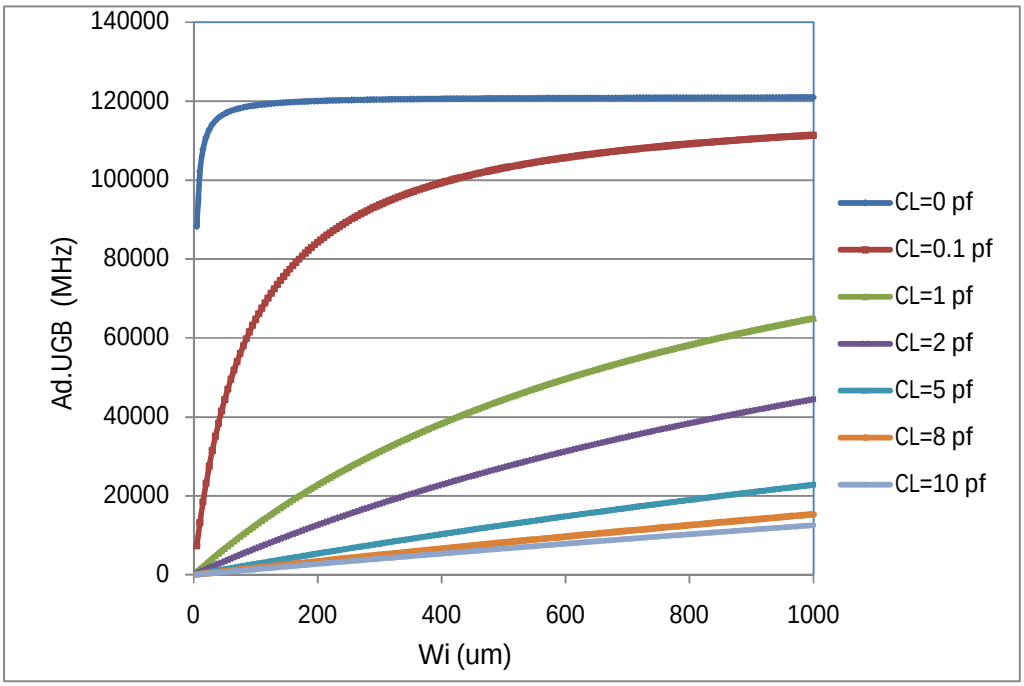


Figure 6.16 Analytical Ad*UGB product variation with external load C_L for MCNC 1.25 μm CMOS technology.

6.6 Layouts and Their Simulations

The layouts of five differential amplifiers were made in the given technology (MCNC 1.25 μm) chosen from the various synthesized circuits. They varied from each other in the widths of the input transistors, W_i = 200 μm, 100 μm, 50 μm, 20 μm, 10 μm. One such schematic and one associated layout corresponding to W_i = 200 μm are shown in Figs. 6.17 and 6.18.

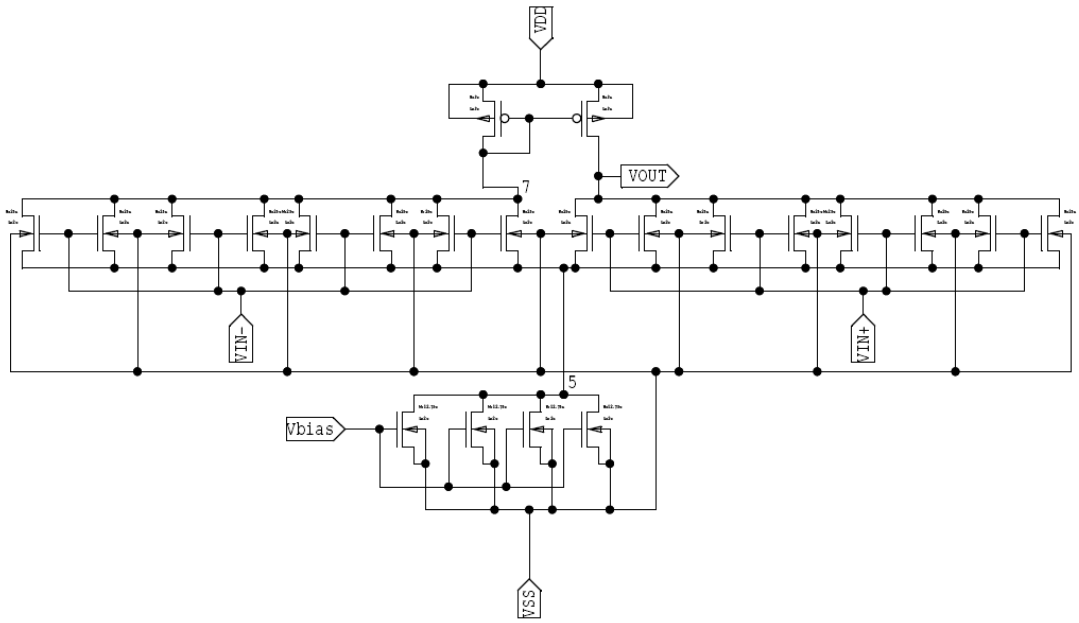


Figure 6.17 Fingered schematic of a Differential Amplifier with W_i = 200 µm.

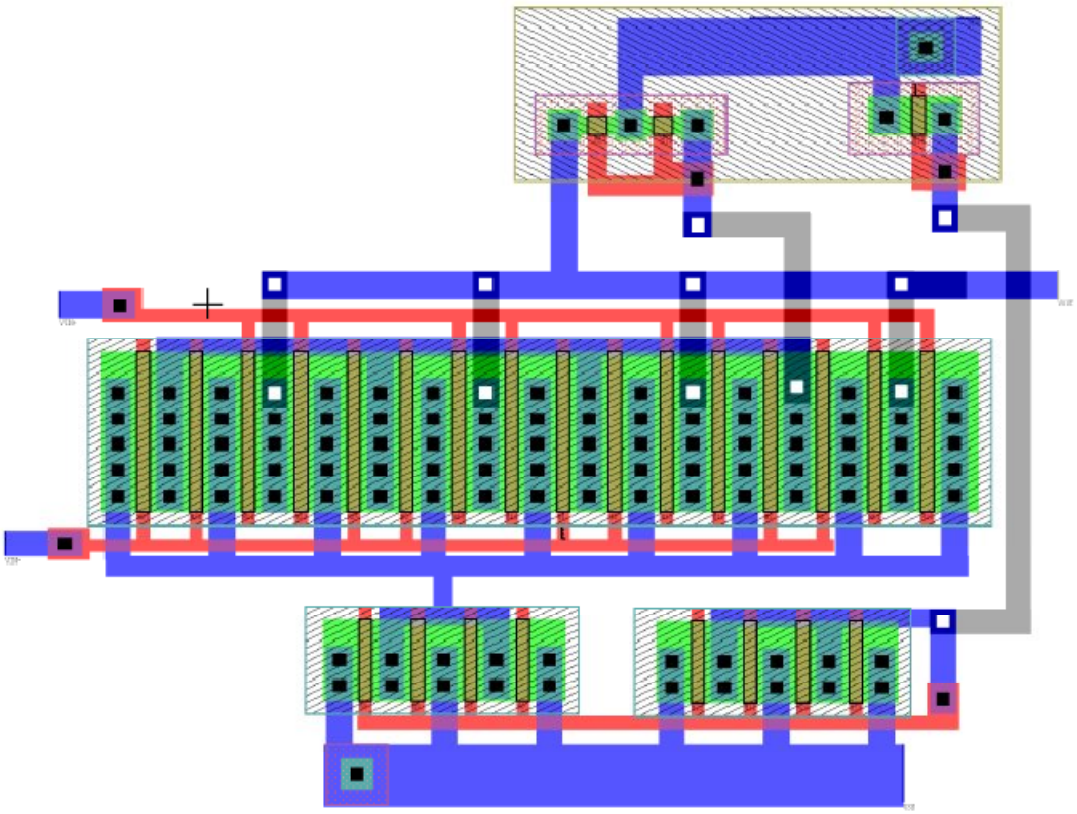


Figure 6.18 Layout of a Differential Amplifier with W_i = 200 µm.

The values of differential dc voltage gain, Unity-gain bandwidth and input referred noise for the schematics and layouts are compared as shown in Figs. 6.19, 6.20 and 6.21. The obtained values are in close match.

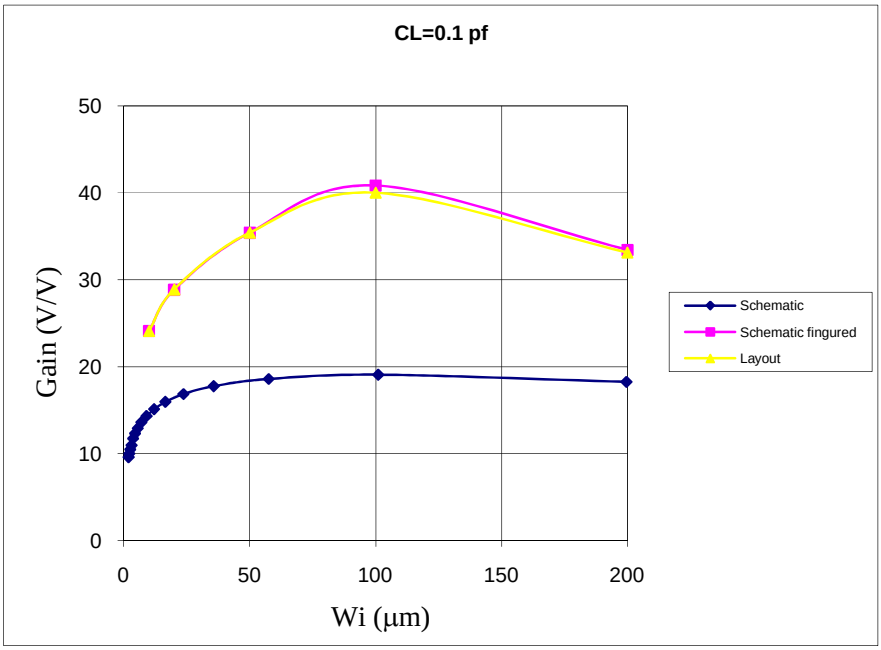


Figure 6.19 Differential dc voltage gain at an external load of 0.1 pf.

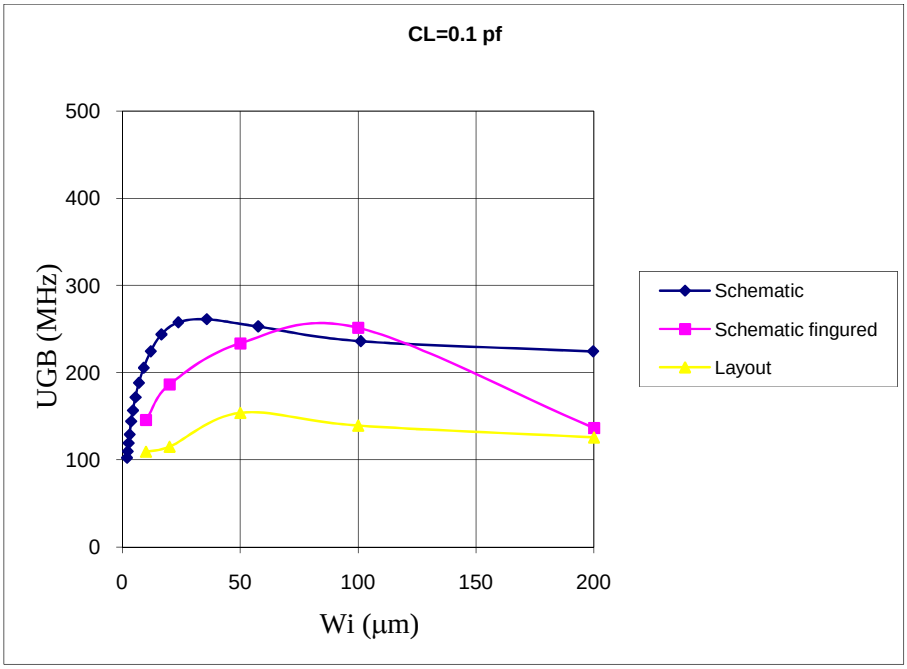


Figure 6.20 Unity-gain bandwidth at an external load of 0.1 pf.

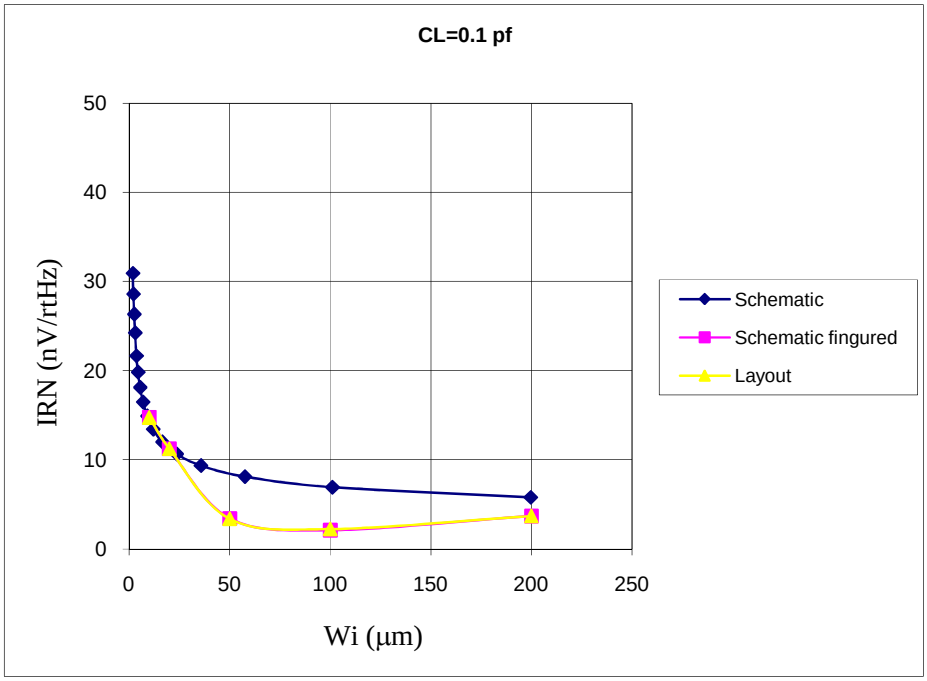


Figure 6.21 Input-referred noise at an external load of 0.1 pf.

The product $Ad \cdot UGB$ obtained from Figs. 6.19 and 6.20 is plotted in Fig. 6.22.

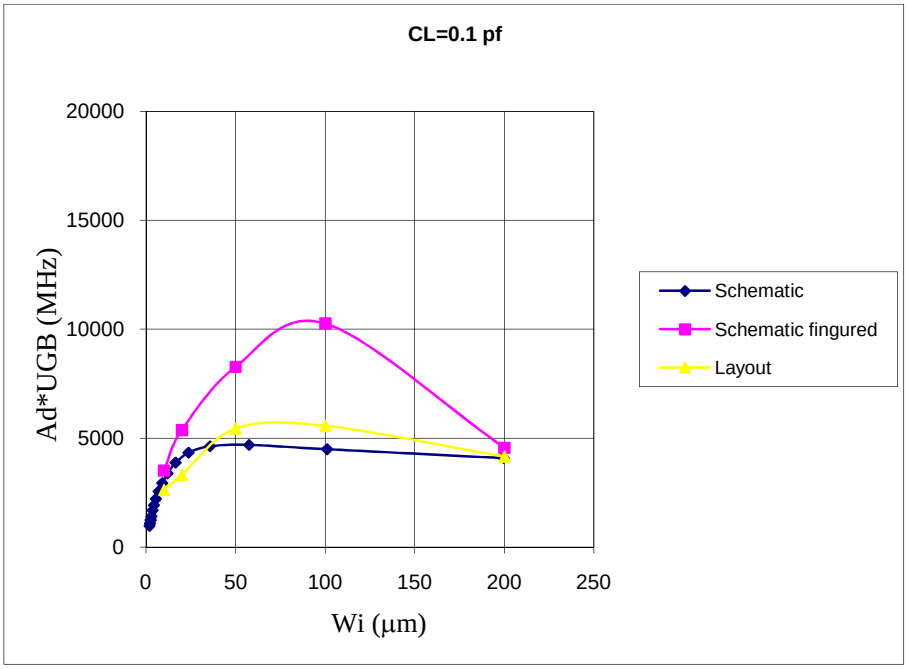
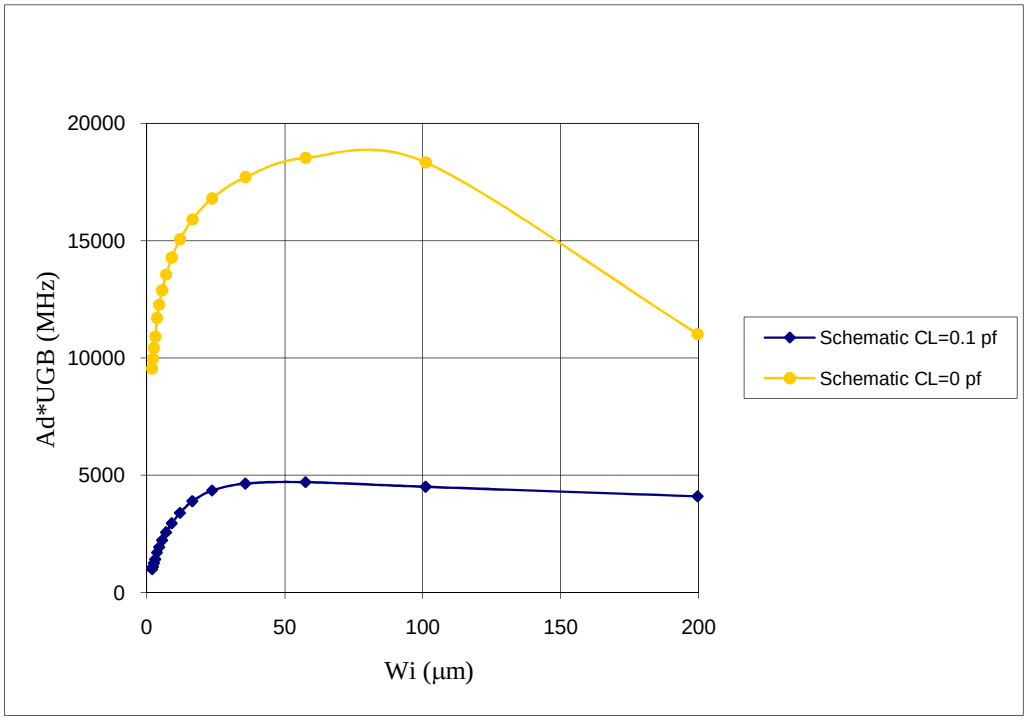


Figure 6.22 Product $Ad \cdot UGB$ at an external load of 0.1 pf.

The product $Ad \cdot UGB$ varying with the applied external load, C_L from schematics and layouts in the given technology are shown in Figs. 6.23 and 6.24.



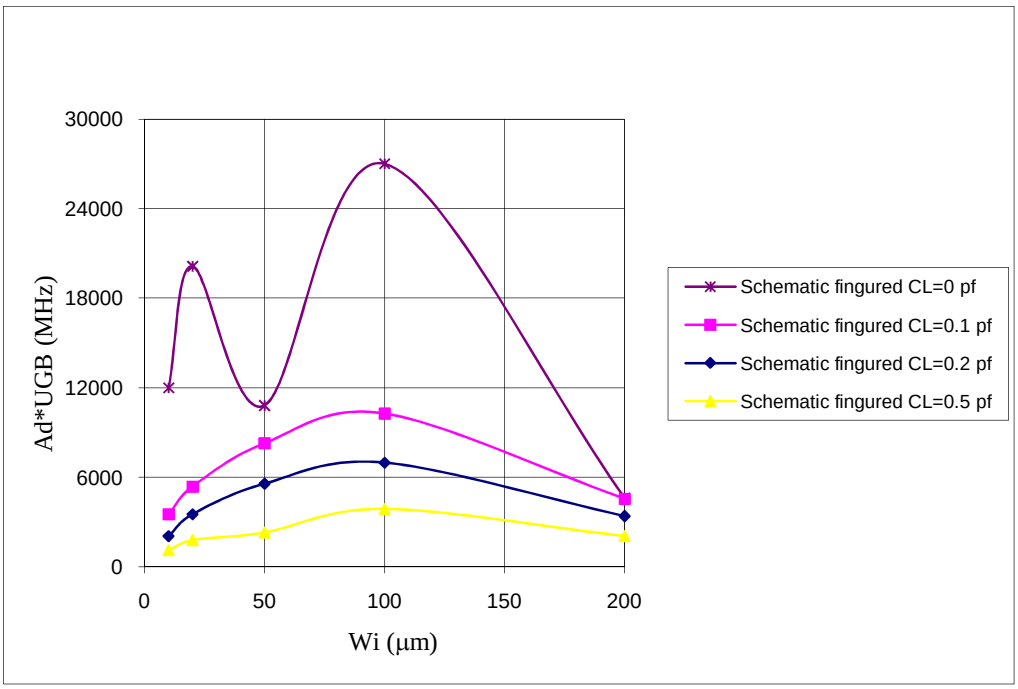


Figure 6.23 Product $Ad \cdot UGB$ varying with external load.

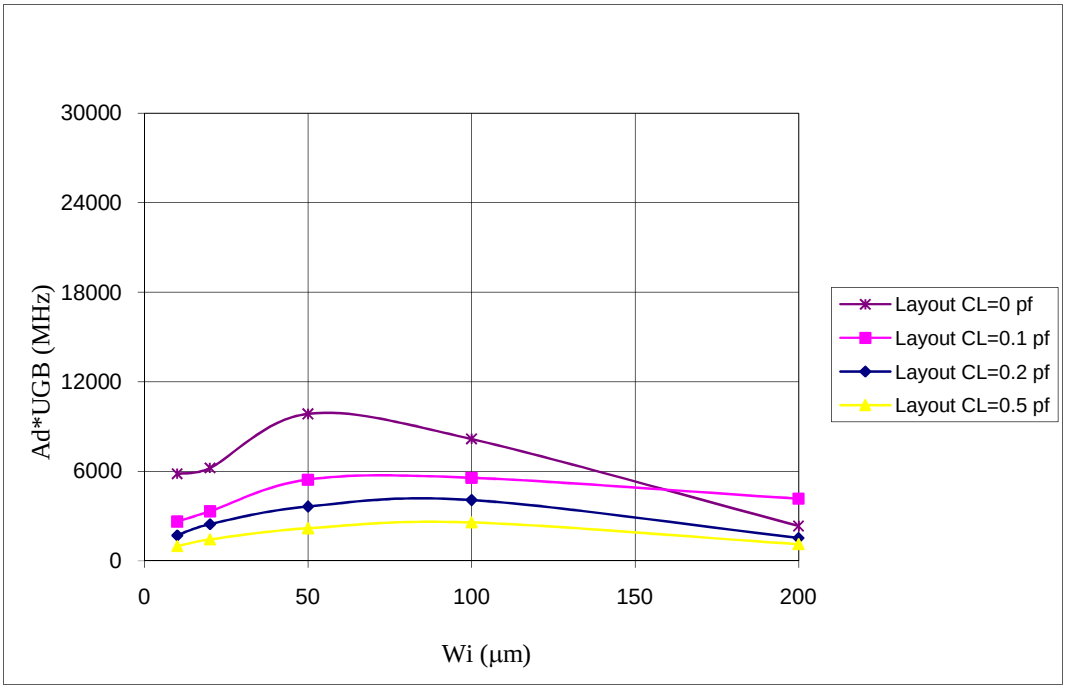


Figure 6.24 Product $Ad \cdot UGB$ from layouts with an external load.