3.1. Introduction

In addition to above listed ABBs, the differential current conveyor (DCCII) was introduced in 1996 (H.O. Elwan et al, 1996) as the first current-mode active element with current differencing capability. However, in the literature it has not received as much as attention than the conventional CDBA presented in 1999 (C. Acar et al, 1999). In fact, the DCCII combines the simplicity of the classical CCII (A. Sedra et al, 1970) with current differencing feature of the CDBA. Therefore, the DCCII looks like a CDBA for current differencing operation, but it has an additional voltage terminal like CCII, which has high-input impedance and can be useful for cascading VM circuits. In addition, the DCCII includes fewer numbers of transistors than CDBA, which has a supplementary voltage buffer stage.

3.2. DCCII Applications

New CMOS realization of high performance differential current conveyor (DCCII) is presented. Presented high performance differential current conveyor is a useful analog building block with the advantage of wide bandwidth. It can be directly used with MOS transistors operating in the ohmic region to implement some essential analog functions. In this study, to increase the variety of DCCII circuits in the literature, its novel implementations using different configurations of DCCII are presented. DCCII is used for realizing many applications viz. Filters, Oscillators, Sine Wave Generators, Square Wave Generators, Current Comparators, Inductance Simulators, Multipliers, Frequency dependent negative resistance (FDNR), Frequency Compensation Circuits.

3.3. All-pass Filters Using DCCII

In the existed literature till now there are three all pass filter circuits are existed and among those three, two circuits are realized using voltage mode approach and the third one is realized in current mode approach. The all-pass filter circuit using single DCCII, two resistors and a single capacitor is shown in Figure 3.1 (B. Metin et al, 2012).
Fig. 3.1. The first-order all-pass filter employing a DCCII (B. Metin et al, 2012). Its voltage transfer function can be expressed as:

\[
\frac{V_0}{V_i} = \frac{2 + 2sCR_1 - sCR_2}{2 + 2sCR_1}
\]  

(1)

Here it should be emphasized that the presented circuit has resistors in series to its X terminals. Hence, by selecting sufficiently high values of \(R_1\) and \(R_2\) the unwanted effects of the parasitic resistors at the X terminals to the operation and resistor matching condition of the circuit can be easily compensated. The simulation shows that the current gain of the DCCII a bit alters from \(\alpha_p\) while the voltage gains \(\beta_N\) and \(\beta_P\) are equal. The \(f_{3dB}\) frequency of voltage transfers is significantly higher than cut-off frequency of the current transfers. The equivalent input and output noises at are found as 43.29 and 39.37 \(\text{nv/}\sqrt{\text{Hz}}\), respectively. This circuit has the inconsistencies in magnitude and phase because of non-idealities existed.

The current mode as well as voltage mode all-pass filter circuits using single DCCII, two resistors and a single capacitor is shown in Figures 3.2 and 3.3 (Emre Arslan et al, 2016). A novel translinear loop based, high performance Complementary Metal-Oxide-Semiconductor (CMOS) second-generation differential current conveyor (DCCII) is introduced. By using super source follower transistors, very low equivalent impedances are obtained at input terminals \(X_N\) and \(X_P\). In addition, new voltage-mode (VM) and current-mode (CM) first-order all-pass filters (APFs) are proposed to highlight the performance of the designed CMOS DCCII.
Fig. 3.2. First-order voltage-mode AP filter.

\[
T_{VM}(S) = \frac{V_{out}}{V_{in}} = \frac{sCR - 1}{sCR + 1}
\]  \hspace{1cm} (2)

\[
T_{CM}(S) = \frac{I_{out}}{I_{in}} = \frac{sCR - 1}{sCR + 1}
\]  \hspace{1cm} (3)

Hence, their sensitivities to passive elements are unity in relative amplitude.

The proposed VM APF in Figure 3.2 has high input impedance and CM circuit in Figure 3.3 has high output impedance. Hence, both proposed APFs have the advantage of being cascadable, i.e. there will be no need for additional voltage buffer or current follower in case of their connection into a voltage or current-mode signal processing channel, respectively.

Note that at high frequencies the deviations in gain and phase characteristics are affected by the poles of voltage and current gains as well as by the external terminal parasitics of the readily available ICs. Moreover, according to datasheets, the
passive element tolerances of selected discrete components are 2% and 5%, which may also affect the precision of \( f_p \).

### 3.4. DCCII Based Band-Pass Filter

As the applications of the presented DCCII, a mixed mode second order band-pass filter is presented by S. Ciftcioglu et al, 2005.

![Fig. 3.4. A mixed mode second order band-pass filter.](image)

The circuit shown in Figure 3.4 represents a mixed mode second order band-pass filter based on the DCCII. Transistors \( M_{11}, M_{12}, M_{21}, \) and \( M_{22} \) are operating in the ohmic region with their nonlinearities canceled out as discussed in the next section of 3.8. The input to this filter section is a voltage while the output is a current and the transfer function is given by:

\[
\frac{I_{BP}}{V_i} = \frac{G_1 G_2}{s^2 + \frac{G_1}{C_1} + \frac{G_2}{C_1 C_2}}
\]

(4)

Where,

\[
G_1 = K_1 (V_{G11} - V_{G12})
\]

(5)

\[
G_2 = K_2 (V_{G21} - V_{G22})
\]

(6)

It is then shown the properties of the block are suitable for designing current mode circuits using CMOS technology.
3.5. DCCII Based Multiple Output Filter

This proposed filter has a low voltage (±1.5V) low power (800µW) multiple output filter performing low-pass, band-pass, high-pass and all pass functions. The filter has been implemented using improved differential second generation current conveyors (DCCIIs) and MOS resistive circuits (MRC) instead of resistances. Thanks to the improved topology of the DCCIIs, the proposed solution allows both to perform the fully integration in a standard CMOS technology and to have the angular frequency and the quality factor easily tunable with excellent agreement of theoretical behavior. Moreover the proposed filter presents low active and passive component sensitivities.

![Diagram of the proposed filter with improved DCCII and MRC.](image)

Fig. 3.5. The proposed filter with improved DCCII and MRC.

The proposed second-order multifunction filter is shown in Figure 3.5. Routine analysis of Figure 3.5 circuit gives the following voltage transfer function:

$$
V_0 = \frac{s^2 C_3 + sG_3 + G_4 G_5}{s^2 + \frac{G_3}{C_2} + \frac{G_4}{C_1 C_2}}
$$

(7)

Where

$$
G_i = \frac{I_{1i} - I_{2i}}{V_{1i} - V_{2i}}
$$

(8)
Where $G_i$ is the conductance of the i-th MRC. The bi-quadratic transfer function can be obtained considering that the output current of each DCCII depends on the output currents of MRC connected at input nodes, so specialization of the numerator in Equation (7) gives the different suitable transfer functions and filter functionalities.

![MOS Resistive Circuit](image)

Fig. 3.6. MOS Resistive Circuit.

It does not employ external resistor and Q-factor and angular frequency $\omega_0$ can be tuned electronically by adjusting the conductance of the MRC. These characteristics make this filter very suitable for a complete on chip integration.

### 3.6. DCCII Based Current Comparator

Comparators are most significant part of analog integrated circuits after operational amplifiers (R. Gregorian et al, 1999, G. Palumbo et al, 1999). Current mode approach advantages lead to current comparator interest in integrated circuit. Differential current conveyor II (DCCII) is designed, modified, and exploited as a comparator with reduced propagation delay and power consumption. New DCCII decreases propagation delay and increases comparator accuracy considerably.

The current comparator concept as expressed by H. Lin et al, 2000 and shown in Figure 3.7 is as follows; the input current is injected into input stage and is converted to the voltage $V_{IN}$ and $V_1$ by amplifier $A_I$ and voltage buffer $A_2$. $V_1$ is amplified using the high gain amplifier ($A_3$) to generate the output logic voltage level. A modified DCCII is used as input stage of the new proposed current comparator due
to the low input impedance at current nodes $X_1$ and $X_2$, and the inherent current to voltage conversion property of the DCCII circuit.

![Diagram](image)

**Fig. 3.7.** Current comparator concept model.

Due to a two gate stage design, the comparator could operate appropriately in low voltages applications. In addition, circuit could be enhanced by replacing ordinary current mirrors with Wilson current mirror and other alternative and prevalent current mirrors (B. Sedighi et al, 2007, S.J. Azhari et al, 2011, B. Razavi et al, 2001) to obtain accurate current copies and higher output impedances while low voltage operation decrease significantly. Wilson current mirror that function well at all current levels, ranging from weak inversion to strong inversion. Also can operate on a low power-supply voltage of a diode drop plus two saturation voltages and features a wide output-voltage swing with cascode-type incremental output impedance. In order to unify output resistance, two inverters are added at the output stage. Therefore, output parasitic impedances are restricted by $r_o/2$ and boosted by enlarged transistor’s length.

### 3.7. DCCII Based Inductance Simulator

In the literature several lossless (pure) synthetic inductance simulators have been proposed since direct physical implementation of inductors on an integrated chip may not satisfy performance requirements of the circuits in comparison to resistors and capacitors in the integrated circuit (IC) realization point of view. For example, they have larger chip area than other passive circuit elements when high inductance values are needed. Therefore, during last few decades the design of synthetic inductors has received considerable attention. The most famous inductance simulators were proposed by Ford and Girling et al, 1966 and A. Antoniou et al, 1969, respectively.
In this study, a differential current conveyor (DCCII) (Elwan and Soliman, 1996) implementation is introduced with two new inductance simulator circuit examples. The proposed circuits enjoy compensating for the effect of the parasitic resistors \( R_X \) at X-terms of the DCCII. Like other inductor simulators that include minimum number of elements in literature, the presented circuits require a resistor matching condition. However, the \( R_X \) parasitic resistors may not affect the resistor matching condition since both resistors in our circuits are in series to the X-terms.

(a) (b)

Fig. 3.8. The proposed grounded inductance simulator circuits.

The admittance transfer functions of proposed circuits in Figure 3.8(a) and (b) are given, respectively, for the ideal case \( (\beta_1=\beta_2=1 \text{ and } \alpha_N=\alpha_P=1) \) as follows

\[
Y_a = \frac{1}{R_2 - R_1 + sCR_1R_2} \quad (9)
\]

\[
Y_b = \frac{1}{sCR_1R_2} + \frac{R_2 - R_1}{R_1R_2} \quad (10)
\]

Equations (9) and (10) illustrate that Figure 3.8(a) simulates serial combination of \( L \) and \( R \) with \( R_S=R_2-R_1 \) and \( L_{eq}=sCR_1R_2 \) and Figure 3.8(b) simulates \( L \) and \( R \) in parallel with \( R_P=R_2+R_1/(R_2-R_1) \) and \( L_{eq}=sCR_1R_2 \). However, pure inductance circuits can be obtained using resistor matching conditions, since it is possible to match resistors with much better precision than 0.1% even in the IC technologies of two decades ago (Gray and Meyer, 1993). For resistor matching condition of \( R_1=R_2=R \), we obtain
\[ Y = \frac{1}{sL_{eq}} = \frac{1}{sCR^2} \] (11)

In this study a novel inductance simulator circuit is presented. The circuit employs minimum number of elements such, e.g. single differential current conveyor (DCCII), one capacitor and two resistors. The proposed circuit can easily be made electronically tunable by means of one of the resistors is replaced by a MOSFET based tunable resistor (Z. Wang, 1990).

![Diagram of proposed inductance simulator circuit using single DCCII, single capacitor, and two resistors.]

Fig. 3.9. The proposed inductance simulators realized using single DCCII.

The proposed circuit for realizing grounded inductor simulators is shown in Figure 3.9. A routine analysis of the input transfer function is given for the ideal case \((\beta_1 = \beta_2 = 1 \text{ and } \alpha_N = \alpha_P = 1)\) as follows:

\[ Y = \frac{1}{sL_{eq}} = \frac{1}{sCR_1R_2} \] (12)

In this study, the usefulness of the DCCII is shown on six novel lossless grounded inductance simulator circuits. Proposed circuits simultaneously employ minimum number of elements, i.e. single DCCII, one capacitor, and two resistors. No passive element matching restriction is needed and all solutions are electronically tunable in case that one of resistors is replaced by MOSFET based voltage-controlled resistor.

The proposed circuits realizing grounded inductor simulators employing single DCCII, single capacitor, and two resistors are shown in Figures. 3.10 (a)-(f).
Fig. 3.10. Proposed lossless grounded inductance simulators using single DCCII.

Considering ideal DCCII ($\beta_N=\beta_P=1$ and $\alpha_N=\alpha_P=1$), routine circuit analyses yield the following input impedance for all six variants:
Passive sensitivities of the proposed circuits are \[ |S_{C,R,R,C}^{L_{eq}}| = 1 \]

![Grounded resistor using two MOSFETs and two symmetrical power supplies.](image)

3.8. **DCCII Based Four Quadrant Multiplier**


A new wideband BiCMOS differential current conveyor is presented by Hesham F. Hamed et al, 2001. The proposed differential current conveyor has the advantage of a wide bandwidth (about 1GHz). It can be directly used with MOS transistors operating in the ohmic region to implement the required analogue functions. As an application of the proposed (DCCII) a four quadrant current multiplier is presented using differential current conveyor.
Some multipliers use the quadratic relation between drain current and gate source voltage of the MOS transistors in the saturation region and others use the MOS transistors in the ohmic region. The proposed differential current conveyor can be used to realize multiplier/transconductance cells. A four quadrant multiplier is shown in Figure 3.12 and consists of a differential current conveyor and two MOS transistors operating in the ohmic region.

\[ I = K(V_G - V_Y)(V_D - V_S) + a1(V_D^2 - V_S^2) + a2(V_D^3 - V_S^3) + \ldots \]  \hspace{1cm} (14)

From the characteristics of the differential current conveyor, \( V_{x1} = V_{x2} = V_Y \) and \( I_z = I_{x1} - I_{x2} \). Transistors \( M_1, M_2 \) have equal drain and equal source voltages by the action of the DCCII. The output currents \( I_{out1} \) and \( I_{out2} \) under the condition that \( M_1 \) and \( M_2 \) are matched are given by:

\[ I_{out1} = I_{x1} - I_{x2} = K(V_{G1} - V_{G2})(V_1 - V_2) \]  \hspace{1cm} (15)

\[ I_{out2} = I_{x2} - I_{x1} = K(V_{G1} - V_{G2})(V_2 - V_1) \]  \hspace{1cm} (16)
The presented DCCII can be used to realize multiplier/transconductance cells as shown in Figure 3.13. The transconductance multiplying action is achieved by the transistors M1 and M2 which are operating in the ohmic region (H.O. Elwan et al, 1996, M. Ismail et al, 1994). The configuration shown cancels both the even and the odd nonlinearities as discussed next.

The current in the ohmic region is given by:

$$ I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + ...... $$  \hspace{1cm} (17)

Since transistors M1 and M2 have equal drain and equal source voltages by the action of the DCCII therefore the output current $I_Z = I_{X1} - I_{X2}$ is given by:

$$ I_Z = K(V_{G1} - V_{G2})(V_1 - V_2) $$  \hspace{1cm} (18)

Thus the cells can be used as a four quadrant multiplier/transconductance.

### 3.9. DCCII Based FDNR Circuit Application

A new CMOS high performance dual-X second-generation current conveyor (DXCCII) is presented. The proposed DXCCII provides good linearity, high output impedance at Z terminals, and excellent output–input current gain accuracy. Besides the proposed DXCCII circuit operating at a supply voltage of ±1.5 V. Moreover, a tunable novel lossless frequency-dependent negative resistance (FDNR) circuit employing only a single active element and three passive components is firstly proposed in this study.

The FNDRs are useful elements for the synthesis and design of active filters. The second generation current-conveyors are very attractive for the realization of

![Diagram of proposed FDNR realization using a single DXCCII.](image)

**Fig. 3.14.** Proposed FDNR realization using a single DXCCII.

![Diagram of proposed tunable MOSFET-C realization using a single DXCCII.](image)

The tunable version of the presented FDNR using MOSFET-C technique is shown in Figure 3.15.

The impedance transfer function is given for the ideal case \( \beta_1 = \beta_2 = 1 \) and \( \alpha_n = \alpha_p = 1 \) for \( C_1=C_2=C \) as follows:
\[ [Z] = \frac{1}{S^2 D_{eq}} = \frac{2}{s^2 C^2 R} \]  

### 3.10. DCCII Based Frequency Compensation methods

A new frequency compensation scheme using a second generation differential current conveyor (DCCII) for three-stage amplifiers is proposed. By adding a DCCII as a feedback path from output of the second and the third stage to the output of the first stage, feed-forward path and the right-half plane zero will be removed subsequently which improves phase margin and the gain-bandwidth product.

To this end, compensation of three-stage amplifiers, Where the amplifier is made up of three gain stages and the second is the only inverting one, the most appropriate solution is the reversed nested Miller compensation (RNMC) (G. Palumbo et al, 2002, R.G.H Eschauzier et al, 1995). RNMC amplifier usually has a better bandwidth than an amplifier with the traditional nested Miller compensation, because the inner compensation capacitor does not load the output node (R.G.H Eschauzier et al, 1995). Nevertheless, conventional RNMC amplifiers are not suitable for low power applications because of their undesired higher order right-half plane (RHP) zero which cause extra power consumption or stability problems. So many RNMC techniques have been reported to cancel the RHP zero (A.D Grasso et al, 2010, K.P Ho et al, 2003, F. Zu et al, 2005, A.D Grasso et al, 2007, A.D Grasso et al, 2004). The presented compensation technique which uses a DCCII block to remove the feed-forward path and the RHP zero thereupon.

In the most of compensation techniques such as NMC and RNMC, compensation network is a feedback and feed-forward path simultaneously. The feed-forward path provides RHP zero, which degenerate frequency response and phase margin mutually. Removing the feed-forward path without attenuation of the feedback can be a solution to obtain suitable frequency response. Voltage and current buffer without influencing feedback path block the feed-forward path and remove undesirable RHP zero completely. However, it is more suitable to use one stage block in the path of Miller capacitors to attain both amplifying feedback and attenuating feed forward path, but the main problem is that the increase in power consumption for adding two blocks is not reasonable. To this end, instead of using two amplifiers or buffers, we can use one DCCII stage in order to buffer two feedback paths and remove
feed-forward. Also it is characterized by transfer function that double pole-zero cancellation occurs that increases the phase margin and gain-bandwidth product.

\[
\frac{H_{ol}}{A_{dc}} = \frac{A_{dc}}{s^2 + a_1 s + a_2} \quad (21)
\]

\[
A_{dc} = g_{m1}r_1 g_{m2}r_2 g_{m3}r_3
\]

\[
a_1 = C_L g_{m2} g_{m3} r_2 r_3
\]

\[
a_2 = C_L C_1 g_{m2} r_1 r_2 r_3
\]

According to denominator of open loop transfer function, amplifier has a dominant pole and a non-dominant pole as \(P_1\) and \(P_2\).

\[
P_1 = \frac{1}{C_{C1} g_{m2} g_{m3} r_2 r_3} \quad (22)
\]

Fig. 3.16. Proposed Compensation Topology.

Figure 3.16 shows linear model of proposed technique. By applying node rule on this model can obtain transfer function of amplifier. In order to reasonably simplify transfer function, the following conditions are assumed:

\[
g_{m1}r_1 \gg 1, \quad C_L \gg C_{C1}, C_{C2} \gg C_1, C_2, C_3
\]

(20)
\[ P_2 = \frac{C_{c1}g_{m3}}{C_{c2}C_L} \]  

(23)

And the gain bandwidth product is defined as follows:

\[ GBW = A_{dc} \cdot P_1 = \frac{g_{m1}}{C_{c1}} \]  

(24)

3.11. Summary

The introduction of various applications using DCCII as the main active element is given in this chapter. The development of many core applications of the electronic industry are given by using the DCCII viz. all pass filters, band pass filters, multiple output filter, current comparator, inductance simulator, four quadrant multiplier, frequency dependent negative resistance circuits, frequency compensation methods.