CHAPTER II
SECOND GENERATION DIFFERENTIAL CURRENT CONVEYOR (DCCII)

2.1. Introduction

The first generation current conveyor (CCI) was presented by Sedra and Smith in 1968. They presented the second generation current conveyor in 1970. However, a certain work to show that the current conveyor was a more advantageous device than the operational amplifier, couldn’t be done during following ten years. So, the current conveyor has been a conceptual device until early 1980s. After innovations in integrated circuit (IC) technology it is that the current conveyor can be realized in ICs. In the result of these works, it was understood that the circuits which are implemented by using CCIIs have their own advantages. Generally, many circuit blocks can be implemented using CCIIs which is easier than implementation using Op-Amps.

The differential current conveyor (DCCII) is a powerful current-mode building block with properties that make it very suitable for designing all-MOS analog circuits which can be integrated on a single chip. The proposed analog block is an extension to the second generation current conveyor presented by Sedra and Smith (A. Sedra et al, 1970). Although the CCII can be used for the realization of many analog functions, the circuits employing the CCII often rely on floating resistors and capacitors which, when integrated on the chip, bring many problems associated with parasitics, area consumption, temperature dependency, etc. The presented differential current conveyor, on the other hand, can be used with MOS transistors operating in the ohmic region to implement the required analog functions where the even and in some cases the odd nonlinearities associated with the transistors operating in this mode can be cancelled out.

2.2. CMOS Second Generation Differential Current Conveyor (DCCII)

The DCCII representation of inputs and outputs with corresponding current direction is shown in Figure 2.1. DCCII is a four terminal device among $Y$, $X_P$ and $X_N$ drives, input and the remaining $Z$ terminal serve as output. The fundamental property of DCCII is current differencing, which is reflected across $Z$ for the input current flowing across $X_P$ and $X_N$. Furthermore, it offers a high input impedance feature which
plays a vital role in the voltage cascading applications, is driven by terminal $Y$ across the input. The potential applied across $Y$ terminal is being copied to the other input terminals of $X_P$ and $X_N$.

\[ \begin{bmatrix} V_{XN} \\ V_{XP} \\ i_Z \\ i_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & \vdots \\ 0 & 0 & 1 & \vdots \\ 1 & -1 & 0 & \vdots \\ 0 & 0 & 0 & \vdots \end{bmatrix} \begin{bmatrix} i_{XP} \\ i_{XN} \\ V_Y \end{bmatrix} \]

(1)

From (1), it has been observed that the output current $i_Z$ is reflected as the difference of input currents $X_N$ and $X_P$, respectively. Along with the same input potential at the $Y$ is driving across the remaining two inputs of $X_P$ and $X_N$ without passing any current through it.

The behavioral model of the DCCII active element is given in Figure 2.2.
2.2.1. Hassan O. Elwan DCCII, 1996

The differential current conveyor (DCC) is a five terminal analog building block as shown in Figure 2.3 with a describing matrix of the form

\[
\begin{bmatrix}
V_{X1} \\
V_{X2} \\
I_{Z1} \\
I_{Z2} \\
I_Y
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 1 \\
1 & -1 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{X1} \\
I_{X2} \\
V_{Z1} \\
V_{Z2} \\
V_Y
\end{bmatrix}
\]  

(2)

![DCC Diagram]

Fig. 2.3. The differential current conveyor.

The MOS realization of the DCC is shown in Figure 2.4. All transistors are assumed to be operating in the saturation region with the sources connected to their substrates. The Y terminal voltage is applied to the gate of transistor M$_1$ along with M$_2$, which forms a CMOS pair. The current through this pair is mirrored by M$_3$, M$_4$ and M$_8$ to the CMOS pairs formed by M$_5$, M$_6$ and M$_{12}$, M$_{13}$ and since the gate voltage of M$_2$, M$_5$ and M$_{12}$ are the same therefore:

\[
V_{X1} = V_{X2} = V_Y
\]  

(3)

The negative feedback operation of the transistors M$_7$ and M$_9$ with the bias currents flowing through transistors M$_{10}$ and M$_{11}$ ensure that the voltage at X$_1$ and X$_2$ remain independent of the current withdrawn from the X terminals. The difference between X$_1$ and X$_2$ currents is conveyed to the Z$_1$ terminal by the mirroring action of transistors M$_{14}$, M$_{15}$ and the current mirror formed by transistors M$_{18}$, M$_{19}$. The inversion of this current is obtained at the Z$_2$ terminal by repeating the above circuit with interchanged current mirror transistors.
The above analysis assumes that the sources of the transistors are connected to their substrates. This is necessary, in order to make the threshold voltage constant for all the transistors, however this requires that, the NMOS transistors and the PMOS transistors be separable in different wells. Although twin well CMOS technology is available, it is not a standard VLSI technology. Another disadvantage is that the use of separate wells increases the layout area because every time separate wells are used, guard rings have to surround each well to prevent latch-up.

Fig. 2.4. The DCC Circuit realization (H.O. Elwan et al, 1996).

2.2.2. F Rat Kacar DCCII, 2010

The DXCCII is conceptually a combination of the regular CCII (T. Kurashina et al, 1998) and the inverting current conveyor (ICCII) (H. Traff et al, 1992). The DXCCII symbol is illustrated in Figure 2.5. It has two X terminals, namely \( X_p \) (non-inverting X terminal) and \( X_n \) (inverting X terminal). The \( X_p \) and \( X_n \) terminal currents are reflected to the respective Z terminals, namely \( Z_p \) and \( Z_n \). (It is worth emphasizing that, for this device, there is no direct relation between the \( Z_p \) and \( Z_n \) terminal currents). The terminal relationship of the DXCCII shown in Figure 2.5 can be characterized with the following equations:
Fig. 2.5. The symbol of the DXCCII.

\[ V_{x_p} = \beta_1 V_y, V_{x_n} = -\beta_2 V_y, I_y = 0, I_{z_n} = \alpha_n I_{x_n}, I_{z_p} = \alpha_p I_{x_p}. \] (4)

Where ideally \( \beta_1 = \beta_2 = 1, \alpha_n = \alpha_p = 1 \) and they represent the voltage or current transfer ratios of the DXCCII.

The CMOS realization of the classical DXCCII is shown in Figure 2.6 (H.A Alzaher et al, 2000, G. Ferri et al, 2003). The \( Z_n \) output resistance of the DXCCII can be found as

\[ R_{z_n} = (r_{d14})/\left(r_{d20}\right) \] (5)

Fig. 2.6. Classical dual-X second generation current conveyor (F. Kacar et al, 2010).
The classical DXCCII is expected to have a suitable current and voltage transfer accuracy in most of its applications. However, the output resistance of DXCCII can further be improved to a fairly reasonable level to enable easy cascading of DXCCII based circuits in current-mode operation. To increase the output resistance, a new DXCCII based on using improved active-feedback cascode current mirror (IAFCCM) (F. Kacar et al., 2010) in the output stages of the conveyor is proposed. The proposed high performance DXCCII is shown in Figure 2.7. A major advantage of IAFCCM circuit is that the output conductance and the feedback capacitance are 100 times lower than the standard current mirror circuit (F. Kacar et al., 2010). Although the number of transistors used in the structure of the proposed DXCCII is larger than the classical one, the output resistance of this DXCCII is much higher. From the Figure 2.7, the output resistance at terminal Z of the proposed high performance DXCCII can be calculated as

\[
R_{Zn} = \left[ g_{m24} g_{m22} r_{dt23} r_{ds32} \left( r_{ds22} // r_{ds20} \right) \right] \left[ g_{m32} g_{m30} r_{dt30} r_{ds32} \left( r_{ds30} // r_{ds28} \right) \right]
\]

(6)

Fig. 2.7. The high performance dual-X second generation conveyor
(F. Kacar et al., 2010).
2.2.3. Reza Chavoshisani DCCII, 2011

Equation (7)-(9) and Figure 2.8, demonstrate differential second generation current conveyor (DCCII) block and matrix characteristic, respectively (M. Fakhfakh et al, 2010). Also, matrix characteristic results are shown as following equations:

\[ I_{Z_1} = I_{X_1} - I_{X_2} \]  
\[ I_{Z_2} = I_{X_2} - I_{X_1} \]  
\[ V_{X_1} = V_{X_2} = V_Y \]

Fig. 2.8. DCCII Block representation.

Fig. 2.9. Complete schematic of DCC-CCII (R. Chavoshisani et al, 2011).
Neglecting the mismatch effect of $M_1$–$M_4$ transistors could lead to equal gate-source voltages. As a case in this point, the unity voltage transfer function ($V_X/V_Y$, Equation (9)) is ensured by using differential pair transistors $M_1$–$M_4$. Furthermore, for calculating the $X$ terminal parasitic impedance common small signal model are used. Equation (10) and (11) are the exact and approximate amount of input impedance, respectively. Practically, bias conditions make the transconductance value is about 500 $\mu$V/A and hence a 2 K$\Omega$ input impedance. The mentioned transconductance is justified by $M_7$–$M_8$ and $M_{11}$–$M_{12}$ transistors. In addition, to obtain equal output impedances and full swing in low current two inverters are added to the $Z$ terminals.

$$R_X = \frac{1}{g_{m7}||g_{05}}$$

(10)

$$R_X \cong \frac{1}{g_{m7}}$$

(11)

2.2.4. BJT-DCCII Implementation, Metin DCCII, 2012

DCCII (Elwan and Soliman 1996; Ciftcioglu, Kuntman, and Zeki 2004) is a five-port analogue building block. Considering the non-idealities caused by the physical implementation of the DCCII, it is described with a matrix equation as follows

$$
\begin{bmatrix}
V_{XN} \\
V_{XP} \\
I_{Z+} \\
I_{Z-} \\
I_Y
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & \beta_1 \\
0 & 0 & \beta_2 \\
\alpha_p & -\alpha_N & 0 \\
\alpha_N & -\alpha_p & 0 \\
0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{XP} \\
I_{XN} \\
I_Y
\end{bmatrix}
$$

(10)

Where ideally $\beta_1=\beta_2=1$ and $\alpha_N=\alpha_p=1$ represent the voltage and current transfer ratios of the DCCII, respectively. All current directions are flowing towards the terminals, as shown in Figure 2.10.

The proposed BJT–DCCII implementation is shown in the Figure 2.10. Transistors $Q_1$–$Q_6$ realise mixed translinear loops (A. Fabre 1983) by transferring $Y$-terminal potential to both $X_N$ and $X_P$ terminals. The current source $I_0$ and transistors $Q_7$–$Q_{15}$ provide biasing for the mixed translinear loops. The transistors $Q_{16}$–$Q_{27}$ form a current differencing circuit at the $Z$-terminals from the currents flowing in to the $X_N$ and $X_P$ terminals.
2.2.5. Bilgin Metin DCCII, 2014

The DCCII is a five-terminal analog building block, whose circuit symbol is shown in the Figure 2.11. The difference of the currents at the X_P and X_N terminals is reflected to the Z terminals. The voltage potential of the Y terminal is copied to the X_P and X_N terminals. Considering the non-idealities caused by the physical implementation of the DCCII, it is described with the following hybrid matrix:

$$
\begin{bmatrix}
V_{X_N} \\
V_{X_P} \\
I_{Z+} \\
I_{Z-} \\
I_Y
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & \beta_1 \\
0 & 0 & \beta_2 \\
\alpha_P & -\alpha_N & 0 \\
\alpha_N & -\alpha_P & 0 \\
0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{X_P} \\
I_{X_N} \\
I_Y
\end{bmatrix}
$$

(11)

where $\beta_i$ and $\alpha_i$ for $i=N,P$ represent the voltage and current gains of the DCCII that are ideally equal to unity.

Fig. 2.11. Circuit symbol of the DCCII.
Unlike DCCII design that includes 21 transistors in H.O. Elwan et al, 1996, the DCCII in S. Ciftcioglu et al, 2005 uses 34 transistors. However, it has very high output impedance due to active feed-back cascade current mirrors. In Figure 2.12, as explained in S. Ciftcioglu et al, 2005, the input currents $i_{XN}$ and $i_{XP}$ are applied to the drain of transistors $M_{12}$ and $M_{14}$, respectively. The Y terminal voltage is applied to the gate of transistors $M_2$ and $M_5$. Because $M_1$, $M_2$, $M_5$, and $M_6$ are matched transistors; the voltage at Y terminal is conveyed to the terminals $X_N$ and $X_P$. The difference between the $X_P$ and $X_N$ currents is conveyed to the Z terminals by the mirroring action of transistors $M_{15}$–$M_{18}$ and $M_{19}$–$M_{22}$. Transistors $M_{23}$–$M_{34}$ form the accurate active-feedback CMOS cascode current mirrors of the output stages.

![Fig. 2.12. A CMOS implementation of the DCCII (B. Metin et al, 2014).](image)

**2.2.6. Emre Arslan DCCII, 2016**

The developed internal structure consists of a class AB input stage based on high performance translinear loop, where one is a CS stage, and the other is current mirror stage. Compared to the previously published CMOS DCCII implementations (H.O. Elwan et al, 1996, S. Ciftcioglu et al, 2005, B. Metin et al, 2012a, B. Metin et al, 2012b), here proposed circuit has very low equivalent input impedances at both
input $X_n$ and $X_p$ ports and high equivalent impedance at the output port $Z$ due to the used source followers with local feedback.

The novel CMOS structure of the proposed DCCII, which is given in the Figure 2.13, is based on class AB translinear loop input stage formed by transistors $M_1$–$M_4$, while CS and current mirror stages are consist of transistors $M_{11}$–$M_{17}$, $M_{19}$, and $M_{18}$; $M_{20}$–$M_{24}$, respectively. Transistors $M_6$, $M_7$ and $M_9$, $M_{10}$ have equal currents and both pairs serve as DC current sources for the translinear loop. Transistor pair $M_2$ and $M_{11}$ forms the source follower with local feedback so-called super source follower (SSF) to obtain very small equivalent resistance at port $X_n$ with other SSF pair $M_4$ and $M_{12}$. Other SSF pairs of transistors $M_{14}$, $M_{17}$ and $M_{15}$, $M_{19}$ are used to obtain very small equivalent resistance at port $X_p$. Current mirror pairs $M_{21}$, $M_{18}$ and $M_{24}$, $M_{20}$ are used to obtain the difference current at output port $Z$.

The equivalent resistance seen on port $y$ of class AB input stage is equal to

$$R_y = \left( \frac{1}{g_{m1} + r_{09}} \right) \left( \frac{1}{g_{m1} + r_{06}} \right)$$

(12)

where $g_{mk}$ and $r_{ok}$ are transconductance and output resistance of $k$-th MOS transistor, respectively. The equivalent resistance seen on ports $x_n$ and $x_p$ are equal to (E. Arslan et al, 2013):

Fig. 2.13. The proposed high performance CMOS DCCII (E. Arslan et al, 2016).
Finally, the equivalent resistance seen on port z can be calculated simply as

\[
R_z \approx \frac{r_{18}r_{20}}{r_{18} + r_{20}}
\]

hence, from output resistance of transistors M_{18} and M_{20}.

2.2.7. Sajjad Shahsavari DCCII, 2015

Proposed technique requires a DCCII block. A typical differential current conveyor that uses two second generation current conveyors depicted in Figure 2.14 (G. Ferri et al, 2003, A. Smith et al, 1970, H.B Gabbouj et al, 2008). As illustrated in Figure 2.14, two CCII form a DCCII where their Y terminals connect to each other and X terminals are triggered with input current source. Also, Z terminals are connected with subtractor input terminals. Current subtractor subtracts out-put currents of each CCII, \(I_{\text{out}}=I_+-I_-\). Figure 2.15 shows the circuit of a second generation current conveyor.

![Current Subtractor Diagram](image)

\(\text{Fig. 2.14. A Block diagram of differential current conveyor.}\)

This type of current conveyor describe by a matrix which is pointed in Equation (16).
\[
\begin{bmatrix}
I_y \\
V_x \\
I_z
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 \\
1 & 0 & 0 \\
0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
V_y \\
I_z
\end{bmatrix}
\]

(16)

From above matrix, it is obvious that X terminal is low impedance node, Y and Z terminals are high impedance nodes. Current of Z terminal is equal to X terminal. By employing second generation current conveyor, both inputs of DCCII are low impedance nodes that do not cause low frequency poles.

Fig. 2.15. Circuit of second generation current conveyor (G. Ferri et al, 2003).

2.2.8. Montree Kumngern DCCII 2014

The symbol of DCCII is shown in Figure 2.16. The ideal DCCII can be characterized as

Fig. 2.16. Circuit Symbol of DCCII.
\[
\begin{bmatrix}
V_{x1} \\
V_{x2} \\
I_{z1} \\
I_{z2}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 1 & -1 \\
0 & 0 & -1 & 1 \\
1 & -1 & 0 & 0 \\
-1 & 1 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{x1} \\
I_{x2} \\
V_{x1} \\
V_{x2}
\end{bmatrix}
\]

(17)

Ideally, the terminals \(Y_1, Y_2, Z_p\) and \(Z_n\) possess high impedance level where as the terminals \(X_p\) and \(X_n\) possess low impedance level for DCCII. Figure 2.17 shows a new low-voltage (LV) low-power (LP) DCCII using bulk-driven and quasi-floating-gate techniques. The differential input stages are consisted of three differential amplifiers. Each differential amplifier uses the BD-QFG MOS transistor technique (F. Khateb et al, 2013). The operation of a BD-QFG MOS transistor can be explained by \(M_1, M_{b2}\), and \(C_1\). \(M_{b1}\) is operated as cut-off region to create a large resistance value. The input signal will excite via \(C_1\) to the quasi-floating-gate from one side and directly couple to the bulk terminal from the other side. The BD-QFG-MOS transconductance is given as \(g_{m,BD-QFG}=g_{mb}+g_{m, QFG}\) (F. Khateb et al, 2013). Hence, the transconductance of BD-QFG-MOS transistor is higher than the BD MOS transistor. The minimum needed power supply voltage can be given by \(V_{DD(min)}=V_{GS(M7,M8,M9)}+V_{DS(M10,M11,M12)}\). The transistors \(M_1\) to \(M_6\) will operate as weak inversion if the voltages \(V_{GS}\) are less than their threshold voltages. Transistors \(M_{19}, M_{20}, M_{21}, M_{10}, M_{11}, M_{12}, M_{28}\) and \(M_{29}\) act as a multiple output current mirror for applying the constant current source \(I_B\) to each branch of the circuit. The power consumption of the proposed circuit can be obtained appropriately by setting the biasing current \(I_B\). Transistors \(M_{10}, M_{11}\) and \(M_{12}\) are common for all differential input stages and they form the active load for them. Transistors \(M_7, M_8\) and \(M_9\) act as tail current sources for all differential input stages. The second stage of three differential input stages is created by cascode transistors \(M_{14}, M_{16}, M_{18}, M_{21}\) and \(M_{22}, M_{24}, M_{26}, M_{28}\). The cascode transistors are used to ensure that the unity gain connection between the outputs of the second stage \(x_1\) and \(x_2\) terminals \((V_{y1}-V_{y2}=V_{x1}-V_{x2})\) can be achieved. On the other hand, the cascode transistors \(M_{13}, M_{15}, M_{17}, M_{20}\) and \(M_{23}, M_{25}, M_{27}, M_{29}\) create the output stage for BD-QFG DCCII at the outputs and they provide the current copies of the \(X_1\) terminal to the \(Z_1\) terminal and the \(X_2\) terminal to the \(Z_2\) terminal.
2.2.9. Sinem Ciftcioglu DCCII 2005

The differential current conveyor is a four-terminal analog building block as shown in Figure 2.18. Describing matrix of the DCCII is given in equation (1).

The MOS realization of the DCCII is shown in Figure 2.19. All transistors are assumed to be operating in the saturation region.
\[
\begin{bmatrix}
V_{X1} \\
V_{X2} \\
I_{Z1} \\
I_{Z2} \\
I_{Y}
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 1 \\
1 & -1 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{X1} \\
I_{X2} \\
V_{Z1} \\
V_{Z2} \\
V_{Y}
\end{bmatrix}
\]

(18)

As shown in the Figure 2.19, the input currents \(I_{X1}\) and \(I_{X2}\) are applied to the drain of transistors \(M_{12}\) and \(M_{14}\), respectively. The Y terminal voltage is applied to the gate of transistors \(M_2\) and \(M_5\). As \(M_1\), \(M_2\), \(M_5\) and \(M_6\) are matched transistors, the voltage at Y terminal is conveyed to the terminals \(X_1\) and \(X_2\). The difference between the \(X_1\) and \(X_2\) currents is conveyed to the Z terminals by the mirroring action of transistors \(M_{15}-M_{18}\) and \(M_{19}-M_{22}\).

\(M_{23}-M_{34}\) transistors form the accurate active-feedback CMOS cascode current mirrors of the output stages. Active-feedback CMOS cascode current mirrors have very accurate current reflection ratio, while achieving high output impedance. Thus they can be used in high precision analogue integrated circuits, especially in structures where current mode techniques are used (A. Zeki et al, 1998).

Fig. 2.19. Proposed CMOS DCCII Realization (S. Ciftcioglu et al, 2005).
2.2.10. Hesham F. Hamed DCCII 2001

The differential current conveyor (DCCII) is an analog building block consists of three input terminals (X₁, X₂ and Y) and two output terminals (Z₁ and Z₂). It can be described by the following matrix:

\[
\begin{bmatrix}
V_{X1} \\
V_{X2} \\
I_{Z1} \\
I_{Z2} \\
I_y
\end{bmatrix} =
\begin{bmatrix}
0 & 0 & 0 & 0 & 1 \\
0 & 0 & 0 & 0 & 1 \\
1 & -1 & 0 & 0 & 0 \\
-1 & 1 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0
\end{bmatrix}
\begin{bmatrix}
I_{X1} \\
I_{X2} \\
V_{Z1} \\
V_{Z2} \\
V_y
\end{bmatrix}
\]

(19)

The MOS realization of the DCCII is shown in Figure 2.20. All transistors are assumed to be operating in the saturation region with their sources connected to their substrate.

As shown in the Figure 2.20, the input current (Iₓ₁) is applied to the drain of the transistor M₃ and the current (Iₓ₂) can be applied to the drain of the transistor M₃₃. The current mirror of the transistors Q₁ with Q₂ and Q₂₂ are connected to convey the voltage at port (Y) to the terminals (X₁) and (X₂).

A level shifter is connected to improve the input current swing. It is composed of two transistors Q₄ and M₅ for the input current (Iₓ₁), and Q₄₄ and M₅₅ for the input current (Iₓ₂). The current mirror, that consists of M₅ and M₆, conveys the input current (Iₓ₁) to the output terminal, and in the same way the input current (Iₓ₂) is conveyed by the current mirror that consists of M₅₅ and M₆₆.

Transistors M₁₁ and M₁₂ compose a current mirror and are connected to have an output current opposite to the input current (Iₓ₁). The current mirror of M₁₁₁ and M₁₁₂ is connected to have an output current opposite to the input current (Iₓ₂). Finally the conveyed currents can be subtracted by connecting the current mirror of transistors M₅₇, M₆₆. The output current is as follows:

\[I_{out} = I_{M6} - I_{M66}\]

(20)

\[= \left( I_{x1}^{-} \right) - \left( I_{x2}^{-} \right)\]

(21)

In the same way, an opposite output current can be obtained from the current mirror of transistors M₁₅ and M₁₆. The output current will be as follows:
\[ I_{out2} = I_{M12} - I_{M112} \]
\[ = (I_{x1}) - (I_{x2}) \]

Fig. 2.20. The differential current conveyor (H.F. Hamed et al, 2001).

### 2.3. DCCII Implementation Using AD844AN

The second generation differential current conveyor can also be implemented using the commercially available IC called a current feedback operational amplifier (CFOA) AD844AN (Y. K. Lo et al, 2007, Y. K. Lo et al, 2007, Y. K. Lo et al, 2006, R. Pandey et al, 2011). The CFOA is a three terminal active device. The circuit symbol of the CFOA is shown in the Figure 2.21 (AD844 Data sheet). The DCCII implementation using the IC AD844AN is shown in the Figure 2.22. Two AD844AN ICs are used to construct the DCCII.

Fig. 2.21. CFOA (AD844AN) circuit symbol.
The DCCII don’t contain any voltage buffer. Therefore, connecting W terminal of CFOA1 to “-” of CFOA2 (instead of Z to “-” as it is in the proposed designs) realizes different from proposed circuits. In other words, in the above mentioned case simulated and realized circuits are not identical. Using the buffer of CFOA2 will not modify the mathematical model of the proposed circuits and will have positive effect as the circuits are able to design fully cascadable applications.

![Diagram of DCCII](image)

Fig. 2.22. Experimental setup of DCCII using AD844AN.

Here in this context it should be noted that the output circuitry of CFOA is voltage buffer. Hence, by using the full potential of the CFOA2, the proposed circuits have both high-input and low-output impedances, simultaneously.

![Diagram of DCCII](image)

Fig. 2.23. The hardware prototype model of DCCII incorporated using AD844AN.

With the schematics shown in Figures 2.22 and 2.23, the proposed circuits in chapter 4 can be implemented on the laboratory bread board to check the theoretical analysis.
2.4. Summary

The evaluation of the current mode devices and in particular the existence of the DCCII for the implementation of various applications are discussed and presented in this chapter. Considering the vital features of the DCCII many researchers introduced various configurations of the DCCII with the existed methodologies. Among all these devices the common and differencing features are explained and the main CMOS realization of the active element is depicted with the relevant information.