CHAPTER V

DCCII BASED WAVEFORM GENERATORS AND ALL-PASS FILTERS: SIMULATION RESULTS

5.1. Introduction

In this chapter, the simulation results for the newly proposed circuits in the chapter 4 using single DCCII active elements are given. All the proposed circuits given in chapter 4 are designed using one DCCII along with few passive components. All the proposed circuits are simulated for waveform generation by using the CMOS DCCII shown in Figure 5.1. The CMOS DCCII shown in Figure 5.1 is designed using Cadence 180 nm CMOS model parameters and simulated by using SPECTRE simulation model parameters. For simulation, the supply voltages ± 2.5 V are used for all the proposed circuits.

![Figure 5.1](image_url)

Fig. 5.1. The second generation differential current conveyor circuit diagram.

The transistors widths and lengths used for simulating the CMOS DCCII by Cadence gpdk 180 nm are given in Table 5.1 and the bias current used during the simulation is \( I_0 = 400 \, \mu A \).
The design parameters of CMOS DCCII as shown in Figure 5.1 are tabulated in Table 1.

Table 5.1 The Transistors Aspect Ratios of the circuit shown in Figure 5.1.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>W (µm)</th>
<th>L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M3, M4, M19, M20</td>
<td>50</td>
<td>0.35</td>
</tr>
<tr>
<td>M5-M7</td>
<td>30</td>
<td>2.0</td>
</tr>
<tr>
<td>M12, M13, M16</td>
<td>30</td>
<td>1.0</td>
</tr>
<tr>
<td>M17</td>
<td>50</td>
<td>2.0</td>
</tr>
<tr>
<td>M1, M5, M18, M21</td>
<td>20</td>
<td>0.35</td>
</tr>
<tr>
<td>M8, M9</td>
<td>10</td>
<td>2.0</td>
</tr>
<tr>
<td>M10, M11, M14</td>
<td>10</td>
<td>1.0</td>
</tr>
<tr>
<td>M15</td>
<td>20</td>
<td>2.0</td>
</tr>
</tbody>
</table>

Fig. 5.2. Layout of the DCCII shown in the Figure 5.1.

Figure 5.2 shows the layout of the second generation differential current conveyor of Figure 5.1 with the optimized chip area of 3334.07 µm² and has used three metal layers for making interconnections between nets and instances of circuit, it is designed using Cadence Virtuoso with the help of gpdk 180 nm technology. And its GDSII file has successfully generated by using Cadence Assura with zero violations in
Design Rule Check (DRC), matched Layout Vs Schematic (LVS) and RCX parasitic extraction of resistances and capacitances.

5.2. Square Waveform Generators Using Single DCCII

5.2.1. Simulation Results

5.2.1.1. Proposed Square Waveform Generator 1

The testing of the proposed square wave generator is shown in Figure 5.3 has done by using Cadence spectre simulation model parameters.

\[ R_1 = 50 \, \text{k}\Omega, \quad R_2 = 3 \, \text{k}\Omega, \quad \text{and} \quad C = 100 \, \text{nF}. \]

The measured time period of the output waveform is \( T = 0.86 \, \text{ms} \).

Figure 5.4 depicts the typical output waveforms of the proposed square wave generator with charging-discharging across the capacitor. The taken values of the passive components in faithful output is \( R_1 = 50 \, \text{k}\Omega, \quad R_2 = 3 \, \text{k}\Omega, \quad \text{and} \quad C = 100 \, \text{nF}. \) The measured time period of the output waveform is \( T = 0.86 \, \text{ms} \).
The linear variation of the time period against the variation of capacitor by fixing $R_1 = 50 \, \text{k}\Omega$, $R_2 = 3 \, \text{k}\Omega$ is shown in Figure 5.5. The variation of capacitor value is from 1nF to 0.4 $\mu$F.

Fig. 5.5. The graph of Time period ($T$) Vs Capacitor ($C$) at $R_1 = 50 \, \text{k}\Omega$ and $R_2 = 3 \, \text{k}\Omega$.

Similarly, by maintaining $R_1 = 50\, \text{K}$ and $C = 100 \, \text{nF}$ the variation of the time period against the value of Resistor $R_2$ can be plotted is shown in Figure 5.6.

Fig. 5.6. The graph of Time period ($T$) Vs Resistor $R_2$ at $C = 100 \, \text{nF}$ and $R_1 = 50 \, \text{k}\Omega$.

The variation of the time period against the value of Resistor $R_1$ is shown in Figure 5.7. For this task, $R_1$ varies within the range of a few ohms to few kilo ohms by keeping the other components at $C = 100 \, \text{nF}$ and $R_2 = 3 \, \text{k}\Omega$. 
Fig. 5.7. The graph of time period (T) Vs resistor $R_1$ at $C = 100 \text{nF}$ and $R_2 = 3 \text{k}\Omega$.

For simulation and tunability, the supply voltage of $\pm 2.5 \text{ V}$ has considered with a biasing current of $400 \mu\text{A}$.

5.2.1.2. **Proposed Square Waveform Generator 2**

Using Cadence Virtuoso, Circuit shown in Figure 5.8 is simulated by considering gpdk 180 nm technology spectre files. For these circuits the required supply voltage of $\pm 2.5 \text{ V}$ where as $400 \mu\text{A}$ for bias current are taken.

A linear resistor can be realized by using a parallel connection of two depletion type NMOS transistors operated in the triode region as illustrated in below Figure 5.9 (A. Gökçen et al, 2010). This method cancels out the non-linearity of the MOSFET significantly.
Fig. 5.9. Linear resistor realization using two NMOS transistors.

The simulated outputs of Figure 5.8 proposed circuit, is shown in Figure 5.10. The circuit output is generated with the selected values of $R_1 = 5 \, \text{k}\Omega$, $R_2 = 15 \, \text{k}\Omega$ and $C = 10 \, \text{nF}$.

\[
R = \frac{1}{\mu_n C_{OX} \left( \frac{W}{L} \right) (V_C - 2V_T)}
\]

Fig. 5.10. The output waveform across output and capacitor node of the proposed square wave generator 2.

The linearity of the proposed circuit with respect to the capacitor variation is shown in Figure 5.11. The capacitor is varied from 1 nF to 1 μF by maintaining other two external components at $R_1 = 5 \, \text{k}\Omega$, $R_2 = 15 \, \text{k}\Omega$.

![Fig. 5.11. Time period (T) variation with respect to Capacitor C by forcing $R_1 = 5 \, \text{k}\Omega$ and $R_2 = 15 \, \text{k}\Omega$.](image)
Similarly, the variation of the time period in contrast to $R_2$ for the proposed model is plotted in Figure 5.12. In doing so, the circuit is forced to $R_1$ at 5 kΩ and $C$ at 10 nF.

![Figure 5.12. Representation of Time period (T) Vs Resistor $R_2$ with $C = 10$ nF and $R_1=5$ kΩ.](image1)

In the same way, the response of time period in accordance with $R_1$ for the invented circuits is presented in Figure 5.13. For achieving this, the circuit values are kept at $R_1 = 15$ kΩ and $C = 100$ nF.

![Figure 5.13. Representation of Time period (T) Vs Resistor $R_1$ with $C = 10$ nF and $R_2=15$ kΩ.](image2)
5.2.1.3. Proposed Square Waveform Generator 3

The simulation setup of Figure 5.14 is carried out in Cadence virtuoso using gpdk 180 nm spectre model libraries at ±2.5 V of supply voltage and biasing current of 400 µA are considered.

![Circuit diagram of proposed square wave generator 3.](image)

The resultant simulation output of spectre simulation is presented in Figure 5.14. Design parameters of the proposed structure in order to satisfy the mathematical model and hardware results are $R_1 = 0.5 \text{ k} \Omega$, $R_2 = 10 \text{ k} \Omega$ and $C = 50 \text{ nF}$ respectively.

![The output waveform across output and capacitor node of the proposed square wave generator 3.](image)

The impact of capacitor sweeping on time period is given in Figure 5.16. From this, the circuit’s linearity over the range of capacitance is attained. To acquire this smooth functionality the other parameters of $R_1 = 0.5 \text{ k} \Omega$ and $R_2 = 10 \text{ k} \Omega$ are chosen.
The observation of the time period (T) versus resistor R₂ is shown in Figure 5.17 keeping other passive components at R₁ and C at 10 kΩ and 50 nF, respectively.

In similar to the previous curves, Figure 5.18 presents the left over the depiction of resistor R₁ to the time period by forcing $R₁ = 0.5 \text{ kΩ}$ and $C = 50 \text{ nF}$. 
Fig. 5.18. The graph representing Time period (T) Vs Resistor $R_1$.

5.3. All-pass Filter Circuits

5.3.1. Simulation Results

5.3.1.1. Proposed All-Pass Filter 1

The theoretical model of the proposed circuit is developed in Cadence Virtuoso environment and simulated using spectre model parameters.

![Circuit Diagram](image)

Fig. 5.19. Circuit diagram of proposed All-Pass Filter 1.

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.20.
Fig. 5.20. The simulated response of proposed all-pass filter as shown in Figure 5.19.

For the model shown in Figure 5.19, the designing parameters can be disclosed as equal to passive component are $R_1 = 12.6 \, k\Omega$, $R_2 = 1 \, k\Omega$, and $C_1 = 1 \, \mu F$ and $C_2 = 100 \, pF$. The supply voltage and biasing current for the above mentioned circuit as shown in Figure 5.19 are $\pm 2.5 \, V$ and $400 \, \mu A$ respectively.

5.3.1.2. Proposed All-Pass Filter 2

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.22.

Fig. 5.21. Circuit diagram of proposed All-Pass Filter 2.
Fig. 5.22. The simulated response of proposed all-pass filter as shown in Figure 5.21.

For the model shown in Figure 5.21, the designing parameters can be disclosed as equal to passive component are $R_1 = 24.5\, \text{k}\Omega$, $R_2 = 5\, \text{k}\Omega$, and $C_1 = 100\, \mu\text{F}$ and $C_2 = 10\, \text{pF}$. The supply voltage and biasing current for the above mentioned circuit as shown in Figure 5.21 are $\pm 2.5\, \text{V}$ and $400\, \mu\text{A}$ respectively.

5.3.1.3. Proposed All-Pass Filter 3

The theoretical model of the proposed circuit is developed in Cadence Virtuoso environment and simulated using spectre model parameters.

Fig. 5.23. Circuit diagram of proposed All-Pass Filter 3.

The simulated response of the proposed all-pass section across the input and output terminal is shown in Figure 5.24.
Fig. 5.24. The simulated response of proposed all-pass filter as shown in Figure 5.23.

For the model shown in Figure 5.23, the designing parameters can be disclosed as equal to passive component are $R_1 = 38.6 \, k\Omega$, $R_2 = 1 \, k\Omega$, $C_1 = 1 \, \mu F$ and $C_2 = 100 \, pF$. The supply voltage and biasing currents for the above mentioned circuit as shown in Figure 5.23 are $\pm 2.5 \, V$ and $400 \, \mu A$ respectively.

5.4. Summary

The theoretical development of the proposed circuits mathematical model is constructed using CMOS realization and the same is designed and tested in the cadence virtuoso environment with the usage of gpdk 180 nm technology library files. The proposed circuits shows approximately close values to the analytical model during simulation and the corresponding values and plots are presented in this chapter.