CHAPTER 5

CONCLUDING REMARKS WITH FUTURE SCOPE

5.1 CONCLUDING REMARKS

In this research work, the efficient structures of the frequency synthesizers have been proposed using various techniques. These techniques are used to improve the performance of frequency synthesizers at different frequencies.

A new architecture of the PLL has been proposed to reduce phase noise that finds applications in global system for mobile communication (GSM), modulation, demodulation, clock recovery etc. The transfer functions of individual source noise and output phase noise have been calculated by considering the locked condition of PLL linear model. The phase noise is now reduced to 33.33% at 1 Hz, 7.3% at 100 Hz and 19% at 100 kHz which show improved performance of proposed architecture as compared to existing techniques.

An optimized DDFS utilizing piecewise linear approximation has also been proposed. Proposed technique allows successive read access to memory cells per one clock cycle using time sharing. The output values will be temporarily stored and read at a later time. The reconstructed signal has been obtained from the output of this proposed system which is superior approximation of the preferred signal. As a result, the DDFS only needs to store fewer coefficients and the hardware complexity is significantly reduced by approximately 26.78 %. The emphasis is on designing the ROM compression algorithms along with paradigm equations mandatory to produce the perfect sine wave pattern for given input and output bit size. The work has analyzed the problem related to the most favorable coefficient option & well-organized execution of system with piece-wise polynomial estimation. In this work, a novel ROM elimination technique has been

presented for application in low complex high spectral purity DDFS. Unlike many reported architectures, which used complex circuits to compute sine samples, the proposed technique uses only 32 points from a standard sine LUT with requirement of fewer registers. System complexity has been greatly reduced approximately 16 % by using an efficient phase to amplitude conversion architecture. The technique has been compared with the existing techniques in terms of storage reduction computation and spectral purity. The proposed DDFS has been analyzed using MATLAB. The results obtained show improvement of around 1.43 % in SFDR over existing results.

Moreover, the design technique has been proposed for DDFS system with high spectral purity which has been optimized for speed and phase accuracy using a combination of Lagrange interpolation and quasi-linear methods. Resulting hardware is less complex, primarily because of the use of better parabolic interpolation based on Lagrange's technique and also by using quasi-linear methods. Resulting waveforms further demonstrated accuracy of the design. In continuation of the above work, fractional SDM PLL has been proposed to reduce phase noise that calculates noise contribution of third order modulator. Transfer function of every source of PN and output PN have been derived and calculated. Phase noise is obtained lies in between from -158 dBc/MHz to -169 dBc/MHz at 20 MHz offset by behavioural modeling using CPPSIM simulator. The results obtained show improvement of around 6.5% in phase noise over existing results.

5.2 FUTURE SCOPE

In the aforementioned research work, new architecture of PLL, DDS, and fractional PLL have been proposed and simulated. Lagrange interpolation, quasi linear methods, and other techniques have been presented and implemented which are useful in wireless communication, different standards, and other engineering applications. Complexity in hardware implementation is found to be in trade-off relationship with efficiency of

presented PLL structures. Therefore, the future work includes designing and development of hybrid architecture based low cost, low power, and highly efficient PLLs structures, which can support the high frequency fractional analysis. In future, DDS based PLL hybrid frequency synthesizer can also be designed for high speed communication applications which is the need of current industries.