CHAPTER 1

INTRODUCTION BASED ON LITRETURE REVIEW

1.1 INTRODUCTION

Wireless high speed data communication is experiencing drastic changes in terms of technologies and architectures as the emphasis of designers is to improve the performance of the modern communication system. In dealing with this remarkable development, significant efforts have been made to limit both capital expenditure and operating expenditure of the communication systems.

In the present era, almost all signal processing problems are resolved in digital domain because of the availability of well-known very large scale integrated (VLSI) circuits. These circuits permit us to carry out complex processes in the real time, without knowing restraints of the analog implementations. The operations like signal filtering, locking time, phase /frequency resolution, mixing etc. are carried out in the digital domain, and its analog equivalence conversion can be done. A very significant and fundamental operation in signal processing is frequency synthesis. This research work deals with various frequencies synthesis techniques such as direct digital synthesis (DDS), phase locked loop (PLL), and hybrid PLL. These techniques find applications in radio frequency (RF), wireless communication, decoding, modulation, demodulation etc. These techniques have various parameters like phase, frequency, amplitude, noise, spur, power etc. These parameters are analyzed by various techniques of frequency synthesis.

Frequency synthesizer is a piece of equipment which produces frequencies from a particular source. The output of the frequency synthesis shows stability and accuracy for long time. In analyzing signal, one can determine one or more output from one or many sources.

There are three frequency synthesis techniques that are being currently used throughout the industry to generate sine wave for further analysis. First one is PLL which is widely used in various communication systems including clock signal recovery, modulation, demodulation etc. It is also used in control system as a feedback mechanism to lock the output to input. It gained popularity because of its economic function, simplicity, low power, and high spectral purity.

The other technique is DDS, which comes under the digital signal processing (DSP) discipline, is commonly used to create, modulate, and generate digital signal and sometimes it is used to convert digital signal to analog signal. It also finds applications in industry due to its small size, reliability, low power, fast switching speed, and good frequency resolution. The main advantage of DDS lies in combining it with DSP processor which can control various parameters such as phase and amplitude. It has applications in military radar and other systems. Its other parameters like phase resolution, frequency hopping, and frequency resolution are analyzed to improve performance of communication system.

The last technique is fractional or hybrid PLL which overcomes the limitation of PLL and DDS. It operates as a DDS inside PLL and some time as a feedback input device.

1.2 MOTIVATION OF THESIS

Communication is area of innovation and research, in which high speed is the major constraint to communicate data from one place to another via wired or wireless media. To fulfil demand of high speed internet and cellular phones, wide bandwidth is required. The new techniques and protocols have been proposed to increase bandwidth and to communicate data over media at higher frequencies with high signal accuracy. Considering above requirements, various new techniques and their parameters have been analyzed to fulfil recent industrial demand. The incredible amount of research about PLLs

in the past decade reflects its importance to high-speed communication as well as the large number of challenges that still exist in PLL design and implementation [1].

In this thesis, the primary aim is to design and implement efficient structures for the hybrid PLL. To accomplish this goal, the cost efficiency and optimal performance designing for PLL and DDS are of main concern. Therefore, an exhaustive literature review has been carried out related to the titled work. Abstracts of some of the most relevant researches are reported in the following paragraphs:

In the era of early 1930's, the super heterodyne receiver was generally used in most of the field of radio communication engineering. Edwin Howard Armstrong was one of the contributors in the same field. His contributions are in the field of regenerative feedback circuits, super heterodyne radio receiver, and frequency modulation radio broadcasting system. The tuned radio frequency (TRF) receiver was also invented by Armstrong in 1918. Afterward, regenerative feedback was incorporated into a broad engineering science developed by H. Black, H. Nyquist, H. Bode and others in the period between 1914 and 1945. In advancement of feedback system, PLL technology came in market, which has communicated significantly towards the technology advancement in the communication system in the past 40 years. This technology has become important system component due to its novel integration circuit technology.

Hsich and Hung [2] presented review on basics of various PLLs with their configuration which is useful in communication based applications. In the continuation of the basic detail of PLL, the different types of PLL have been reviewed by Prasad and Sharma in [3]. The problem associated with the different PLL architectures like analog, digital, linear, and all digital have been implemented in Simulink. The author also reviewed PLL techniques, which is applicable to latest day to day application for the communication system. Therefore, Lata and Kumar in [4] presented great contribution in digital

communication. This work provides basic principles and details of each component of digital PLL in control system and digital communication system. The simulation results show the comparative analysis of each component. After reviewing history and basic detail of PLL, other parameters have been analyzed in the next section.

1.2.1 Estimation of phase noise and their reduction techniques of PLL & ADPLL

Smedt and Gielent [5] proposed evaluation of phase noise spectrum. The behaviour modeling has been used for voltage controlled oscillator (VCO) to find highly accurate loop analysis. The authors performed the corroboration between output of spectrum of VCO model and output of transistor level VCO spectrum, in which voltage has been taken as an input. The results were simulated and compared with existing techniques.

Considering the previous work, self injection of VCO has been presented by Chang [6] to minimize noise. This technique was also based on feedback loop analysis. In this case, an elevated Q factor resonator and a time hold-up have been used to illustrate results. The output noise may be diminished at offset frequency in vicinity area of carrier. It also returns to VCO noise when input is zero and far away from carrier with stable loop condition. This technique may be used to reduce the phase noises. Besides phase consideration, frequency locked loop (FLL) is also proposed by Juan et al. [7] to reduce phase noise of wideband VCO. The author derived design equations to reduce noise and find stability of the system. The results showed better performance as compared with the previous techniques. Another wide band voltage locked feedback loop was designed in bipolar complementary metal oxide semiconductor (BiCMOS) [8] and which achieve up to 20 dB reduction of VCO phase noise.

Takagi proposed a new method to reduce phase noise of PLL based on subtraction of correlated noise [9] from its average current noise. The theoretical and experimental results have been compared. This work obtained 7 dB reductions in phase noise

approximately. Another technique which is also used to reduce VCO phase noise is called frequency steered technique. This work presented digital VLSI integrated circuit (IC) technology. The implementation of VCO and analysis of its phase noise characteristics have been done using this technique. The parameters of system were identified and the performance of system has been characterized. The result showed that system can lock easily to confine in particular region of frequency to reduce VCO noise. This technique also allows improvement of poor quality of VCOs for the industrial applications.

Wicpalek et al. [10] presented a frequency discriminator in ADPLLs for radio frequency synthesis to fulfil requirement of industrial applications like global system for mobile-communication (GSM) and universal-mobile-telecommunication system (UMTS). One of the requirements is in-band phase noise performance, which was analyzed theoretically and practically respectively. The results showed improvement in the performance of the PLL. This work was implemented using two bit frequency discriminator in complementary metal oxide semiconductor (CMOS) technology. This discriminator was also used in profitable CMOS Bluetooth radio based applications. The measured phase noise was -86 dBc/Hz for GSM application. The mathematical and operational details of the same have been presented.

Considering other requirements, the minimum acquisition time and maximum noise rejection in the presence or absence of frequency drift has been analyzed by Sandoz and Steenaart [11]. This work proposed a new aided acquisition technique to improve the performance of ADPLL. The numerical values of pseudo-two dimensional random-walk filter and phase error variance were analyzed. These results show comparison between theoretical and experimental analysis, which were very satisfactory. Drift frequency was tracked for feedback modified loop to improve the ability of system. This technique also reduced signal to noise ratio as compared to the other. The phase noise of digital

frequency dividers were investigated by Kroupa in [12] and found good as compared to the previous work [11].

Mishra et al. [13] proposed behaviour and mathematical modeling of PLL at -450 MHz, which is used in various communication applications like frequency synthesizers, computer, radio, clock generator, recovery, global positioning system (GPS), demodulation, etc. This work presents analysis of third order PLL with their industrial applications. The key parameters such as timing jitter, lock time, locking range, and bandwidth are tested and calculated by MATLAB Simulink tool. Timing jitter is the important parameter, which can mortify the response of the PLL. The method was presented for minimization of timing jitter of PLL, in which, two PLLs were connected in cascade form [14], where first one has been used as a voltage controlled crystal oscillator PLL and other used as a wide band PLL to reduce jitter. The simulation results presented better performance as compared with the existing methods.

Signal-to-noise ratio (SNR) and unit interval root mean squared (UIRMS) have been presented in [15] to focus on output jitter of various synchronizers. This work was divided into two groups, the first was filter with carrier PLL and the second was based on symbol PLL. The prototype of each group was analyzed to reduce output jitter of the proposed system. Considering clock recovery, Kim and Kim [16] proposed dual digital PLL (DPLL), which is used in digital transmission to process frequency and phase as input parameters and results showed reduction in substantial jitter and adjust DPLL loop bandwidth accordingly. The work presented adaptive algorithm, which adjusts bandwidth to allow fast acquisition and jitter reduction at various noise environment. This algorithm was based on recursive least square criterion to control parameter of dual loop DPLL. This work achieves fastest acquisition time to minimize jitter at any given time instant.

This short preamble duration is useful in various applications like wireless communication, networks, storage devices etc.

Liao et al. proposed a mitigation technique [17] with laser voltage probing to minimize jitter. This technique presents PLL IC, which has probing circuitry to allow detecting small amount of excess jitter that was masked due to large jitter to detect at output of system. The details of probing setup jitter analysis jitter mitigation methodology and timing measurement were presented in this work. Instead of direct estimation of jitter, an indirect on chip method has been presented in [18] to estimate PLL charge pump (CP) jitter. The spectral purity of the system is an important parameter to measure directly within a production test environment. These sets of work focus a new framework to implement methodology that can detect block level errors and minimize spectral degradation. This provides a platform where jitter is tested on fully embedded CP-PLL. In addition to above frame work, another substrate noise also affected the performance of charge pump. This work was estimated and simulated in 0.15 μm technology. The results showed a reduction of 12.5 dB in the system output spur level at an offset of 5 MHz. The results suggested that mixed signal with other isolation technique are used to reduce noise on radio frequency circuits.

Gao et al. [19] proposed spur reduction technique for the PLL. This technique was based on sampling phase detector, in which clock input was fed to sample signal for VCO. At this reference input, the periodic disturbances of the other sources of VCO were sampled. Dummy sampler and isolation buffer were described to minimize sampling spur of oscillator. The buffer and delay of system were presented to tune frequency to reduce spur level. This design demonstrates effectiveness of spur level, in CMOS technology and its reference spur was around less than -80 dBc, which is used in low bandwidth. Considering above periodic disturbance in oscillator, a new method [20] presented by

Stensby to limit sweep rate of VCO, which is used for serving industrial applications like receivers, transponders, decoders etc. To limit effect of noise, band width of feedback loop should be kept small and make their phenomenon too reliable. The loop frequency error is decreased with sweep voltage. The results analyzed and compared with existing techniques.

Jinghui [21] presented analysis of 5-8 GHz PLL using discrete Z domain. The transfer functions of various order of the PLL in Z domain were presented. Predicted values of jitter were compared with its existing architectures. Considering previous jitter reduction architecture, a new programmable PLL architecture is proposed by Sulaiman et al. in [22], which is implemented on field programmable gate array (FPGA) platform. As programmable architecture designers are free to change their design at implementation level also, so the performance can be improved in various forms such as low output jitter, lower power, and clock control. Finally, architecture presented low power high performance system. Moreover, stability is another constraint to check performance of the system. Paemel [23] described a model to check stability of second order charge pump PLL. There are two conditions to find the stability, first loop is lock and second is loop out of lock. This work presented transient behaviour with its well defined state variables for that particular model. This work determined stability and overloads limits and verified their validity for various applications. Another technique also presented by Tillman and Stensby [24] using various tracking phenomenon, but in this phenomenon, input was taken as a sum of two sinusoidal signals. However, the previous analysis was incomplete and further analysis of the PLL response to the sum of sinusoidal signals was presented. The amplitude ratio and frequency response were defined to track stability of the system.

Gokc et al. proposed an adaptive estimator [25] which is embedded into a conventional PLL. An adaptive frequency estimator was used to predict its performance with the help

of Linear and nonlinear model. These models provide guidelines to designer for increasing efficiency of the system. The results showed improved performance for the same. Another adaptation method presented by Roche et al. in [26], which is used to minimize error and maintain stability using locking phenomenon and loop bandwidth of the system. The charge pump current is controlled by adaptive technique to enhance loop bandwidth. After analysis, the phase error, loop bandwidth, and locking status were achieved. This work was simulated and implemented in CMOS technology. Unwanted signal was the main constraint, which was introduced in feedback loop, described by Saito et al. [27]. This work was presented to alleviate concerned clock pulse, which was generated due to unwanted signal. This clock pulse controls whole process without timing skew. The large incident noise was also realized by adding filters. The validity of stable system was determined using simulation results.

Moreover, analog analysis, digital frequency steering method [28] has been implemented by Hill and Cantoni to stabilize the system. In this method, frequency of closed loop has been compared with reference input and applied to VCO to control stability. The output recognized disturbances of digital frequency steering loop. These disturbances and errors have been rectified using this method. This work was implemented for high speed clock information recovery and compared with existing techniques.

Hanumolu et al. [29] proposed an impulse invariant transformation method, which is used to determine state variables and state equations for analysis of tracking behaviour. This method described lock acquisition process and linear behaviour of large and small signal respectively. The noise transformation and state equations were derived to realize linearization method for signal conditions. An impulse invariant transformation method was analyzed and compared with existing methods. Also, feedback loop parameters like frequency and phase, with their effects on phase margin and stability have been derived

and analyzed. The results were verified by simulation tool MATLAB. Moreover stability, transient characteristics like locking time, output jitter, capture, and locking ranges are presented by Chan et al. [30]. This work used bang-bang type PLL, which described behaviour model. Result showed how the application of this model in a simulator can speed up simulation time by four to five orders of magnitude. The simulation results were analyzed and compared with conventional methods.

Considering previous work, Stork [31] proposed a novel architecture in the form of digital components that can be used to enhance performance of the PLL. This design consists of up-down counter, shift registers, and frequency generators, which are an appropriate design to find stability and used it for other applications like frequency synthesizer, clock recovery etc. But this architecture is limited to low frequency base applications, so these limitations can be overcome using fractional frequency synthesizer. The detailed analysis of PLL and fractional PLL are described and compared to stabilize the system.

Kumm et al. [32] also proposed a new algorithm for digital PLL and its implementation on FGPA to enhance the performance. All digital components have been realized with their functions and parameters have been derived for analysis. Besides digital system, the coordinate rotational digital computer (CORDIC) algorithm and Hilbert transforms are used to unwrap phase component for extending range. This work maintains locking time for frequency changes and also analyzed frequency and stability range with their processing delay. All transfer functions and details of each components of system were derived. Finally, Zhang et al. [33] presented research and application of ADPLL for the communication system. This work also provides time domain analysis of each digital components of ADPLL. Mathematical models of the first and the second order systems have been presented using linear approximation method. These results were simulated by XILINK and implemented on FGPA platform. This architecture can also be used in an

inductive heating system, control system, and other communication system. In this section, it has been found that these techniques are not suitable to overcome phase noise of the PLL at higher order. Therefore, it is essential to comprehend and quantify jitter so that their outcomes on upper stage artefact are reduced. The effects of these noises should be minimized using various PLL configurations and also with the effect of poles and zeros of the filters with the same.

1.2.2 Efficient Implementation of Piecewise and Lagrange Interpolation Methods of Direct Digital Synthesis

Direct digital synthesis (DDS) is another type of frequency synthesizer, which is used in low power, fast switching speed, and good frequency resolution based applications. Larson [34] described and compared theoretical and practical analysis of various parameters. The limitations of traditional analogy PLL are overcome by proposed architecture. The results show that this architecture is useful for high speed communication. Considering previous work, Caro and Strollo [35] proposed a new technique that used piecewise polynomial approximation. This method analyzed error, SNR, and spur free dynamic range (SFDR). The polynomial reduced effort to maximize the SFDR with the help of coefficients. The quadratic and piecewise linear methods have been realized to design the proposed system. Conventional and proposed techniques have been discussed and compared. The results showed reduced area and less complexity of the system. The performance can also be improved after combining width arithmetic and single summation tree architectures. The results obtained show that piecewise quadratic design is more effective than piecewise linear design to measure SFDR. Generally third order system is used to design good DDFS in terms of SFDR. Another piecewise continuous linear interpolation method is proposed by Langlois and Khalili in [36]. In this method, sine function is approximated with desired linear segments to fulfil the

requirements of memory storage and computational complexity. The number of linear segments and resolution of slope are correlated with each other to achieve desired output. The memory storage requirements of proposed DDFS were identified and implemented. Considering the previous work, read only memory (ROM) less quadrature DDFS was presented in [37]. Because of ROM look up table (LUT), it was very difficult to store huge amount of data in conventional system. To avoid this problem, low power ROM-less technique was used to design suitable system for portable wireless communication applications. Mortezapour and Lee also proposed [38] a new ROM less DDFS using digital to analog converter (DAC). Here, ROM LUT was replaced with nonlinear DAC for conversion of phase to sine amplitude. Two quadrature DDFS were used to implement the proposed system. This work was demonstrated and implemented by nonlinear resister strings DAC and current mode DAC both. The results found that there are around 4 mW and 92 mW power dissipation for non linear resister string DAC and current mode DAC respectively. Instead of two DACs, this work described [39] low power DDFS with an on chip DAC. This technique included accumulator, two phases to sine converters and DAC. This parallelism method increases conversion process for high speed operation of the system. Inter-chip interconnection helped to save delay and power consumption in the on chip DACs. This technique was implemented in CMOS technology. Considering the previous work [35], Ashrafi and Adhami [40] proposed a new model of DDFS. In this work, the first quadrant of a sine signal has been interpolated using even and linear piece-wise parabolic polynomial. These techniques found to be helpful to maximize SFDR and solve the problem of complexity of the system. The proposed design is called as quasi linear because the first quadrant of signal is approximated by even parabolic polynomial method. The results showed an improvement in SFDR with respect to existing techniques. Another work presented a smaller LUT for sine function. This function is interpolated

with the help of their coefficient by using piecewise parabolic interpolation method [41]. The results found that ROM size is reduced around 1 K bits at the 80 dBc of SFDR.

Considering the work [37], Saber et al. [42] proposed a new architecture of DDFS based on quadrature piecewise interpolation. This work was employed without ROM as already discussed in [37], but this was implemented on FPGA to avoid high power consumption of the system. This work consumed around 4 mW and SFDR was better than previous work. Considering the previous work, another ROM compression technique of DDFS has been proposed in [43]. The work presented multiple segments piecewise polynomial technique to store values of sine function for the LUT. The phase is mapped with amplitude for the required output bits of the ROM. The results found reduced ROM size and good spectral purity of the signal. The compression ratio was good as compared to other technique. Considering work [37], Khan et al. [44] also proposed ROM less quadrature architecture. This technique reduced the complexity of the system. This ROM less technology was more efficient that existing work [37]. The results showed an improvement in term of area. Another ROM less architecture of DDFS has been proposed by Hegazi et al. [45], which is based on sampling ratio. This technique reduced settling time for the DAC. The results were simulated and compared with existing architectures.

Considering previous work, Vankka [46] presented a new architecture, which was based on mapping of phase to sine amplitude. This mapping increased the resolution of LUT. Bramble [47] also presented a novel technique which is used to convert wave shape of phase accumulator into desired accumulative address of ROM LUT. The limitations of previous work have been eliminated. Various memory compression techniques have been compared.

Nieznanski [48] proposed an alternative approach for the DDS which is the extension of previous work [37]. This approach eliminated pulse position jitter, which also originated

from the accumulator. Besides this low jitter, low power ROM less system has been analyzed by Fahim [49]. Analog interpolation method and circuit topologies were used by Fahim to reduce jitter of the system. This work has been implemented in CMOS technology. Considering low jitter in previous work, the work [50] - [53] also presented low jitter clock of DDFS. This work analyzed phase error that incorporate with time to reduce jitter at the output. Better results have been found in terms of jitter and compared with other existing technologies. In this section, it is found that access to memory cells at specific time is the main cause, so there is need to introduce new technique to access more memory space in less time and minimize noise at high speed for the communication system.

1.2.3 Noise reduction of Hybrid PLL using Sigma Delta Modulator

Fractional PLL is the hybrid frequency synthesizer. It is similar to the divide-by-N PLL. Marques et al. [54] presented an overview of the evolution of fractional PLL. Analog PLL, digital PLL and DDS are having some limitations which are overcome using fractional PLL. The parametric analysis of the fractional PLL has been described by Stork and Kaspar in [55]. In this work, output of the VCO is not restricted to only multiple reference input but also its locking mechanism which is used for the fractional multiples frequency tuning. This frequency has been controlled by predicted value of band width of PLL, at the same pass band. The high frequency and less settling time synthesizers have been analyzed to fulfil the requirements of modern applications. Considering previous work, the various parameters like phase noise, band width, locking time etc. have been analyzed by Riley et al. [56] and Zarkeshvari et al. [57]. This work also described linearity of components and band phase noise of the same. These techniques are useful for recent trend industrial applications. This work also reviewed various techniques of the system with their advantages and disadvantages.

Perrott [58] proposed a modeling approach based on sigma delta modulator (SDM) fractional PLL. This model has been incorporated with fractional divide value for various components. This work analyzed noise and dynamic characteristics of SDM which is implemented in CMOS technology. Another linearization method for a wide band sigma delta fractional PLL has been presented [59]. This work used two techniques; the first one is modulation for noise reduction and the second is charge pump linearization. These techniques have been presented and demonstrated to detect component error and enable them for wide band fractional system based applications. The results obtained were better than previous works.

A linearized charge pump technique to reduce error in the system was proposed by Su & Pamarti [60]. This technique has been divided into two parts; first, suppressed spurious tone and the second reduced phase noise, which occurs due to mismatching of the charge pump process. The theoretical and practical results have been calculated and compared. Zhang et al. proposed finite modulo [61] high order SDM fractional system. This method generates less spur which is achieved by compensating voltage and current in various domain. This work is implemented in CMOS technology and its results are good as compared to previous architectures. Considering previous work, Arora et al. [62] proposed mathematical model of fractional PLL, which determines spur and phase error at the output. This work calculated sources of noise of each component and presented its effects on the output of system. The results showed the comparison of various existing techniques.

A linearized model of the fractional system has also been presented by Venerus & Galton [63] and Jin et al. [64], which is based on sigma delta frequency to digital converter. These techniques determined linearity requirement of system and also resulted in reduction of area. This method also reduced quantization noise of sigma delta modulator

in the feedback loop. It is very difficult to choose correct type fractional SDM PLL to get less noise, high speed, and good frequency resolution. This work has reviewed several systems with its parameters by Kit et al. [65] for the communication system. The results were simulated using CPPSIM simulator. The design parameters such as phase noise, frequency resolution, and settling time have been presented and compared. These parameters already have been analyzed in previous works, but Riley et al. [66] also proposed a new multi-stage noise shaping (MASH) modulation concept, in which low phase noise and fast settling time with their effect on the system, have been presented. Besides [64], Park et al. [67] proposed a novel architecture, which achieves low noise and suppress quantum noise of the sigma delta modulator. This work consumes less power around 32 mW using charge recycling technique, which has been implemented in CMOS technology. Another dual reference frequency technique has been described by Feng [68] to reduce phase noise and spur. This work resulted in better frequency resolution and short locking time, which is useful in wireless communication systems.

Considering references [61] & [64], novel fractional-N PLL architecture has been proposed by Jian et al. [69], which is used for multi band communication using binary weighted differential and offset frequency modulator. Quantization noise and spur are minimized using these techniques. Firstly, binary weighted method has been utilized for mismatched shaping to minimize quantization noise. Secondly, offset frequency modulator has been utilized to reduce in-band spur. Yang et al. developed phase compensation technique [70], which can reduce fractional spur of the system. It's operational frequency ranges from 1.5 GHz to 2.7 GHz and found better divide ratio. This work adopted on-chip phase compensation using delay locked loop which is simulated and implemented in CMOS technology with its power dissipation is around 6.9 mW.

Moreover, Richard and Ramaswamy [71] proposed multi-stage noise shaping and single loop modulator which are used for wireless application to reduce spur. These techniques analyzed various parameters to minimize the spur. The parameters have been analyzed and compared with existing techniques. After considering various limitations which were not rectified by analog architecture, all digital fractional PLL has been proposed in [72]. This architecture is an enhanced architecture of the fractional PLL. The main component of this design is dual modulus divider controlled by modulator output which is used to minimize spur level of the system. The results were studied and comparisons were done among various existing techniques. Considering other limitations, which were not overcome by single architecture of PLL or DDS? Then, new hybrid concept came in the market to fulfil such type of requirements. Hu et al. [73] designed a new PLL-DDS-PLL based hybrid architecture for various types of applications. This work described low spurious, which was around 65 dBc. The comparative results were better than previous existing techniques.

The bandwidth is important parameter to improve the performance of fractional PLL. Pu et al. [74] described loop bandwidth of the system to manage jitter and spurious performance. A circuit component is added along signal path which improves bandwidth. The results have been discussed and compared with the conventional architecture. Another work has been proposed by Meninger and Perrott [75], extending bandwidth of the fractional PLL. The issues of bandwidth in term of quantization noise of design have been explained. This model is reframed to analyze system noise to achieve high bandwidth. The methodology has been demonstrated and compared. A new fractional hybrid PLL has applications [76], [77] in both narrower and wider bandwidth which operate in two modes, firstly using integer phase lock and secondly using fractional PLL transient. Fractional PLL achieves fast locking as compared to integer PLL, this fast

locking is benefited in various important applications. This work is implemented in CMOS technology.

Ferriss and Flynn [78] proposed all digital phase detectors, which includes filip-flop. These flip-flops have been used to reduce phase quantization noise using oversampling method. This digital scheme increases modulation rates much larger than loop bandwidth, which determines accuracy of output signal.

Considering previous work, another digital automatic calibration circuit has been embedded in [79], [80]. This work extended oversampling concept which was presented in [77]. This work presented sigma delta modulator for non sinusoidal waveforms. The clock generation and dynamic adjustment of their free running frequency are determined to lock PLL in suitable lock range to find stability of the system. The results are simulated and demonstrated. In previous work, it was described that how to find stability by locking concept. In this work, a novel digital building circuit has been presented by Stork [81] to determine stability of the system. This design includes registers, frequency generators, and other components. This work determines stability and generates pure signals. This architecture is much simpler and suitable to design VLSI based applications. Its advantages, disadvantages and future scope have been presented. Besides VLSI technology, signal processing based applications have been presented by Song and Ignjatovic in [82]. This design includes new threshold DDS based delta modulator. The loop decomposition of sigma delta is configured to increase throughput of modulator. The results found low power fractional-N PLL. Rhee et al. [83] also described aspect of finite impulse response (FIR) with fractional-N PLL. This method describes spur generation and nonlinearity issues of the PLL. This fractional PLL is used in embedded systems.

Fractional synthesizers can be simulated and implemented in various platforms. One of the languages is hardware description language (HDL), which can be used for both

simulation and synthesis. The behaviour modeling on HDLs have been proposed with their applications in [84], [85]. This work described source noise of different components and showed that it affects at output of the PLL. The various specifications of configuration of the system have been described and compared. The results are obtained and compared by VHDL simulation tool and implemented by XILINX tool.

Hybrid architecture of the PLL is very useful to overcome limitations of single PLL and DDS architecture. Considering these limitations, Linn [86] developed hybrid PLL for the communication system. This work presented methodological approach to design and implement hybrid PLL. The various configurations and types of PLL have been presented. Another new DDS-based-PLL has been proposed by Bonfanti et al. [87] to achieve better frequency resolution, fast settling time, and spectral purity. The DDS is used as feedback components with VCO. Output of VCO and DDS are mixed to complete closed path. The complete output of VCO is used to determine spectral purity of the system. This work is implemented and compared with various existing techniques. The different parameters with their configurations have been analyzed. This work finds application in various fields like wireless local area network (WLAN) [88], orthogonal frequency division multiplexing (OFDM) receiver [89], and distributed generator [90]. On the basis of previous literature, it is found that clock plays important role to process information in the communication system. It determines hard and soft variation of input and output of VCO. The small random variation of input voltage of VCO is one of important factors that cause output phase noise. It is necessary to employ a mechanism for smoothing the variations. For smoothing the variation of input voltage of VCO, there is a need to use new technique, which can limit and reduce phase noise of the system. For that a fractional - SDM - PLL can be designed to reduce noise for the better performance of the communication system.

1.3 PROBLEM FORMULATION

The modern communication system is experiencing a rapid expansion. To meet the tough real time requirements posed by modern wireless communication systems, high performance, and low cost signal processing architectures must be developed. The new algorithms and techniques are required to improve system performance while reducing the cost of equipment. One of the important devices of the modern communication system is PLL. The purpose of the PLLs is to increase signal processing speed at low noise. These systems are helpful for the signal analysis, de-noising, compression, and so forth. To consider the increasing cost pressures on many wireless equipment makers, significant efforts are being made to reduce complexity, low noise, high processing speed, flexibility etc. The high speed wireless communication system can be efficiently realized with the help of hybrid PLL. However, the disadvantage of a PLL is that, this technique is not suitable to overcome phase noise of the PLL at higher order. So, there is a need to introduce the techniques which can improve the performance of PLL at the high speed. Another difficulty arises in the DDS to access the memory cells using clock pulse. So, there is need to develop new technique that will allow accessing memory twice at one clock cycle using time sharing at the high speed for the communication systems.

However, the PLL and DDS are unsuitable for those practical applications, where fractional divider value is required at high speed. As an interesting remedy for the problem, the sigma delta modulators are extensively used in practice for attaining the fractional value. The single architecture of PLL and DDS are efficient for communication of low order frequency. For the high order communication, the hybrid PLLs are preferred because single architecture does not offer effective response. However, the hybrid design increases the complexity of the system. For such scenarios, there is need to develop a technique for the efficient realization of the hybrid PLL. Moreover, better design and

implementation of hybrid PLLs can result in low cost and low noise communication system with improved performance.

1.4 RESEACH OBJECTIVES

In the light of aforementioned aspects, the research objectives for the investigation are as follows:

1. To study the existing PLL and DDS techniques.
2. To propose novel algorithm in which PLL & DDS technologies can be conjoined by design of synthesizers to achieve improved performance of PLLs.
3. To implement and validate the proposed system on FPGA platform.

1.5 THESIS OUTLINE

The thesis has been organized in five chapters. The details of the contents of each chapter of the thesis are as follows

- Chapter one presents the introduction and motivation based on the literature survey, problem formulation, objectives of the thesis, and organization of thesis.
- Chapter two describes the parametric analysis to minimize noise of frequency synthesizers for wireless communication systems. The noise contributions of frequency synthesis are described based on presented analysis. The results have been simulated with the help of Agilent's Advanced Design System.
- Chapter three describes DDFS based on piecewise linear approximation, Lagrange interpolation, and modified quasi linear methods. The proposed techniques allow successive read access to memory cells per one clock cycle using time sharing. The desired waveforms have been approximated to get reconstructed signal at the output. As a result, the DDFS technique needs only to store fewer coefficients and the hardware complexity is significantly reduced with its spectral purity. The results have been simulated with the help of MATLAB & impulse C.

- Chapter four deals with the parametric analysis of a novel architecture of fractional PLL for communication system. This work proposed a mathematical model to take care of noise of the components and to calculate predicted noise. Finally, the effect of these noises for the fractional synthesizer has been simulated using CPPSIM.
- Finally, the chapter five sums up the research work. Further, a brief description about the future work/scope has been presented as a motivational seed for the germination of research work. The thesis concludes with the research publications as well as the list of references found useful during the course of investigation.

1.6 SUMMERY OF THE CHAPTER

This chapter acts as a capsule for the motivation of the thesis. An exhaustive literature survey has been presented about phase noise, jitter, area, high speed etc. of PLL, DDS, and hybrid PLL. Based on this, the objectives of the thesis have been identified, in which the main motive is to increase efficiency and to reduce noise, area and complexity of the PLL. In the next chapter, the effects of phase noise of PLL for wireless communication system have been presented.