10.1 Micro controller

10.1.1 Memory Organization

There are three memory blocks. The Program Memory and Data Memory have separate buses so that concurrent access can occur. EEPROM is data memory block.

10.1.2 Program memory organization

The PIC16F877 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. The PIC16F877 devices have 8K x 14 words of FLASH program memory.

10.1.3 Data memory organization

The data memory is partitioned into multiple banks which contain the General Purpose Registers and the Special Function Registers. Each bank extends up to 128 bytes.

10.1.4 Data EEPROM and flash memory

The Data EEPROM and FLASH Program Memory are readable and writable during normal operation over the entire VDD range. These operations take place on a single byte for Data EEPROM memory and a single word for Program memory.

10.1.5 Stack

The PIC16F87X family has an 8-level deep x 13-bit wide hardware stack. The stack space is not part of either program or data space, or the stack pointers are not readable or writable. The PC is PUSHED onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPEd in the event of RETURN, RETLW or a RETFIE instruction execution. The stack operates as a circular buffer. This means that after the stack has been PUSHED eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second.

10.1.6 Program Counter

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The upper bits are not readable, but are indirectly writable through the PCLATH register.
10.1.7 Register

10.1.7.1 Special function register

The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device.

10.1.7.2 General purpose registers

The register file can be accessed either directly or indirectly through the File Select Register (FSR), VDD, and temperature and process variation.

10.1.7.3 Status registers

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bits for data memory. The STATUS register can be the destination for any instruction, as with any other register.

10.2 Features of Microcontroller

The Pin diagram of Microcontroller PIC16F877A is shown in Figure 10.1 and description of Microcontroller PIC16F877A is tabulated in Table 10.1. The Features of Microcontroller PIC16F877A maybe as follows:

- Only 35 singl word instructions to learn
- Operating speed: DC - 20 MHz clock input
- DC - 200 ns instruction cycle
- Up to 368 x 8 bytes of Data Memory (RAM)
- Up to 256 x 8 bytes of EEPROM Data Memory
- Eight level deep hardware stack
- Selectable oscillator options
- Low power, high speed CMOS FLASH EEPROM technology
- Single 5V In-Circuit Serial Programming capability
- Wide operating voltage range: 2.0V to 5.5V
- Direct, indirect and relative addressing modes
- Low power consumption
- High sink Source current: 25mA
10.3 Pin Diagram of Microcontroller PIC16F877A

40-Pin PDIP

MCLR/VPP → 1 → 40 → RB7/PGD
RA0/AN0 → 2 → 39 → RB6/PGC
RA1/AN1 → 3 → 38 → RB5
RA2/AN2/VREF-/CVREF → 4 → 37 → RB4
RA3/AN3/VREF+ → 5 → 36 → RB3/PGM
RA4/T0CKI/C1OUT → 6 → 35 → RB2
RA5/AN4/SS/C2OUT → 7 → 34 → RB1
RE0/RD/AN5 → 8 → 33 → RB0/INT
RE1/WR/AN6 → 9 → 32 → Vdd
RE2/CS/AN7 → 10 → 31 → Vss
VDD → 11 → 30 → RD7/PSP7
VSS → 12 → 29 → RD6/PSP6
OSC1/CLKI → 13 → 28 → RD5/PSP5
OSC2/CLKO → 14 → 27 → RD4/PSP4
RC0/T1OSO/T1CKI → 15 → 26 → RC7/RX/DT
RC1/T1OSI/CCP2 → 16 → 25 → RC6/TX/CK
RC2/CCP1 → 17 → 24 → RC5/SDO
RC3/SCK/SCL → 18 → 23 → RC4/SDI/SDA
RD0/PSP0 → 19 → 22 → RD3/PSP3
RD1/PSP1 → 20 → 21 → RD2/PSP2

Figure 10.1 PIN DIAGRAM OF PIC16F877A
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>DIP Pin#</th>
<th>PLCC Pin#</th>
<th>QFP Pin#</th>
<th>I/O/P</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSC1/CLKIN</td>
<td>13</td>
<td>14</td>
<td>30</td>
<td>I</td>
<td>ST/CMOS(4)</td>
<td>Oscillator input/external clock source input.</td>
</tr>
<tr>
<td>OSC2/CLKOUT</td>
<td>14</td>
<td>15</td>
<td>31</td>
<td>O</td>
<td>—</td>
<td>Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.</td>
</tr>
<tr>
<td>MCLR/VPP</td>
<td>1</td>
<td>2</td>
<td>18</td>
<td>I/P</td>
<td>ST</td>
<td>Master Clear (Reset) input or programming voltage input. This pin is an active low RESET to the device. PORTA is a bi-directional I/O port.</td>
</tr>
<tr>
<td>RA0/AN0</td>
<td>2</td>
<td>3</td>
<td>19</td>
<td>I/O</td>
<td>TTL</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RA1/AN1</td>
<td>3</td>
<td>4</td>
<td>20</td>
<td>I/O</td>
<td>TTL</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RA2/AN2/VR-</td>
<td>4</td>
<td>5</td>
<td>21</td>
<td>I/O</td>
<td>TTL</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RA3/AN3/VR+</td>
<td>5</td>
<td>6</td>
<td>22</td>
<td>I/O</td>
<td>TTL</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RA4/T0CKI</td>
<td>6</td>
<td>7</td>
<td>23</td>
<td>I/O</td>
<td>ST</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RA5/SS/AP4</td>
<td>7</td>
<td>8</td>
<td>24</td>
<td>I/O</td>
<td>TTL</td>
<td>RA0 can also be analog input0. RA1 can also be analog input1. RA2 can also be analog input2 or negative analog reference voltage. RA3 can also be analog input3 or positive analog reference voltage. RA4 can also be the clock input to the Timer0 timer/counter. Output is open drain type. RA5 can also be analog input4 or the slave select for the synchronous serial port.</td>
</tr>
<tr>
<td>RB0/INT</td>
<td>33</td>
<td>36</td>
<td>8</td>
<td>I/O</td>
<td>TTL/ST(1)</td>
<td>RA0 can also be the external interrupt pin.</td>
</tr>
<tr>
<td>RB1</td>
<td>34</td>
<td>37</td>
<td>9</td>
<td>I/O</td>
<td>TTL</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin.</td>
</tr>
<tr>
<td>RB2</td>
<td>35</td>
<td>38</td>
<td>10</td>
<td>I/O</td>
<td>TTL</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin.</td>
</tr>
<tr>
<td>RB3/PGM</td>
<td>36</td>
<td>39</td>
<td>11</td>
<td>I/O</td>
<td>TTL</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin.</td>
</tr>
<tr>
<td>RB4</td>
<td>37</td>
<td>41</td>
<td>14</td>
<td>I/O</td>
<td>TTL</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin.</td>
</tr>
<tr>
<td>RB5</td>
<td>38</td>
<td>42</td>
<td>15</td>
<td>I/O</td>
<td>TTL</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin.</td>
</tr>
<tr>
<td>RB6/PGC</td>
<td>39</td>
<td>43</td>
<td>16</td>
<td>I/O</td>
<td>TTL/ST(2)</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock.</td>
</tr>
<tr>
<td>RB7/PGD</td>
<td>40</td>
<td>44</td>
<td>17</td>
<td>I/O</td>
<td>TTL/ST(2)</td>
<td>RA3 can also be the low voltage programming input. Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data.</td>
</tr>
</tbody>
</table>
10.4 Peripheral Features

- Timer 0: 8 bit timer/counter with 8 bit pre scalar.
- Timer 1: 16 bit timer/counter with pre-scalar, can be incremented via external crystal/clock
- Timer 2: 8 bit timer/counter with 8 bit period register, pre-sealar and post­
  scalar.
- PWM mad. Resolution is 10bit
- 10 bit multi channel Analog to digital converter.
- Universal Synchronous Asynchronous
- Receiver Transmitter (USART) with 9 bit address detection
- Brown out detection circuitry for Brown Out Reset (BOR)
- Parallel slave port (PSP) 8 bits wide, with external RD, WR. CS, controls.

10.5 Analog to Digital Converter module

The Analog-to-Digital (A/D) Converter modules have five inputs for the 2 8-pin devices and eight for the other devices. It is shown in Figure 10.2. The analog input charges a sample and holds capacitor. The output of the sample and hold capacitor is the input into the converter. The A/D conversion of the analog input signal results in a corresponding 10-bit digital number.

The A/D module has four registers. These registers are:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)

10.5.1 Ports in Microcontroller

Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

10.5.2 PORT A and TRISA Register

PORTA is a 6-bit wide bi-directional port. The corresponding data direction register is TRISA. Setting a TRISA bit (=1) will make the corresponding PORTA pin an input. Clearing a TRISA bit (=0) will make the corresponding PORTA pin an output. Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations.
Therefore, a write to a port implies that the port pins are read; the value is modified and then written to the port data latch. Pin RA4 is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output.

![Figure 10.2 Analog to Digital Converter Module](image)

All other PORTA pins have TTL input levels and MI CMOS output drivers. Other PORTA pins are multiplexed with analog inputs and analog VREF input. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register.
10.5.3 PORT B and the TRISB Register

PORTB is an 8-bit wide bi-directional port. The corresponding data direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode).

Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin). Three pins of PORTB are multiplexed with the Low Voltage Programming function: RB3/PGM, RB6/PGC and RB7/PGD. The alternate functions of these pins are described in the Special Features Section.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (OPTIONJREG<7>). The weak pull-up is automatically turned off, when the port pin is configured as an output. The pull-ups are disabled a Power-on R.

10.5.4 PORTC and the TRISC Register

PORTC is an 8-bit wide bi-directional port. The corresponding data direction register is TRISC. Setting a TRISC bit (= 1) will make the corresponding PORTC pin an input driver in a Hi-Impedance. Clearing a TRISC bit (= 0) will make the corresponding PORTC pin an output. PORTC is multiplexed with several peripheral functions. PORTC pins have Schmitt Trigger input buffers. When the I2C module is enabled, the PORTC " 4:3 'i- pins can be configured with normal I2C levels or with SMB user levels by using the CKE bit.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input.

Since the TRIS bit override is in effect while the peripheral is enabled, read-modify write instructions with TRISC as destination should be avoided. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

10.5.5 PORT D and TRISD Registers

PORTD and TRISD are not implemented on the PIC16F873 or PIC16F876. PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTD can be configured as an 8-bit wide microprocessor port (parallel slave port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL.
10.5.6 PORT.E and TRISE Registers

PORT.E and TRISE are not implemented on the PIC16F873 or PIC16F876. PORT.E has three pins which are individually configurable as inputs or outputs. These pins have Schmitt Trigger input buffers. The PORT.E pins become the I/O control inputs for the microprocessor port when bit PSPMODE (TRISE<4>) is set.

In this mode, the user must make certain that the TRISE<2:0> bits are set, and that the pins are configured as digital inputs. Also it must be ensured that ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

Register 3-1 shows the TRISE register, which also controls the parallel slave port operation. PORT.E pins are multiplexed with analog inputs. When selected for analog input, these pins will read as '0's. TRISE controls the direction of the RE pins, even when they are being used as analog inputs. The user must make sure to keep the pins configured as inputs when using them as analog inputs.