LIST OF FIGURES

FIGURE 1-1 IEEE 754-2008 DECIMAL INTERCHANGE FORMATS ................................................................. 9
FIGURE 1-2 IEEE 754-2008 decimal64 decimal floating point format .......................................................... 9
FIGURE 2-1 BLOCK DIAGRAM OF SINGLE DIGIT BCD ADDER ................................................................. 30
FIGURE 2-2 BLOCK DIAGRAM OF CONVENTIONAL SINGLE DIGIT BCD ADDER ........................................ 32
FIGURE 2-3 BLOCK DIAGRAM OF WORD WIDE ADDER (OPERAND SIZE = 2 DIGITS) ................................. 33
FIGURE 2-4 BLOCK DIAGRAM OF WORD WIDE ADDER (OPERAND SIZE = 4 DIGITS) ................................. 33
FIGURE 2-5 BLOCK DIAGRAM OF WORD WIDE ADDER (OPERAND SIZE = 16 DIGITS) ............................... 34
FIGURE 2-6 BLOCK DIAGRAM OF 11:2 COMPRESSOR ............................................................................ 34
FIGURE 2-7 COMPLETE 11 x 16 DIGIT RADIX – 10 FIXED POINT ADDER .................................................. 36
FIGURE 2-8 GRAPHICAL DELAY ANALYSIS FOR CONVENTIONAL BCD ADDER ........................................ 45
FIGURE 2-9 GRAPHICAL DELAY ANALYSIS FOR PROPOSED FAST BCD ADDER ........................................ 50
FIGURE 2-10 THEORETICAL AND HARDWARE COMBINATIONAL PATH DELAY ANALYSIS .......................... 55
FIGURE 2-11 LOGIC TIME ANALYSIS ........................................................................................................ 56
FIGURE 2-12 ROUTE TIME ANALYSIS ........................................................................................................ 57
FIGURE 2-13 NUMBER OF SLICE UTILIZATION ON FPGA .......................................................................... 58
FIGURE 2-14 NUMBER OF LOOK UP TABLE UTILIZATION ON FPGA .......................................................... 58
FIGURE 2-15 NUMBER OF INPUT OUTPUT BUFFER UTILIZATION ON FPGA ............................................ 58
FIGURE 3-1 HIGH LEVEL DIAGRAM OF REDUCED MAGNITUDE PARTIAL PRODUCT GENERATOR ................. 66
FIGURE 3-2 REDUCED MAGNITUDE NIKHILAM MULTIPLIER (BLOCK 32 OF FIGURE 3-1) ............................ 73
FIGURE 3-3 REARRANGEMENT OF MULTIPLICAND AND MULTIPLIER FOR PARTIAL PRODUCT ACCUMULATION USING URDHVA-TIRYAKBHYAM SUTRA ........................................................................ 75
FIGURE 3-4 PARTIAL PRODUCTS ACCUMULATION USING URDHVA TIRYAKBHYAM SUTRA (MATRIX FORM) .................................................................................................................. 78
FIGURE 3-5 A. PARALLEL PATH PARTIAL PRODUCTS REDUCTION FOR CRITICAL PATH COMPONENT ........ 82
FIGURE 3-6 FINAL CARRY PROPAGATION ADDER ARCHITECTURE BASED ON FIGURE 3-5B ......................... 84
FIGURE 3-7 THEORETICAL LOGIC LEVEL VS FPGA SYNTHESIS ANALYSIS (BLOCKS IN FIGURE 3-1) .......... 94
FIGURE 3-8 LOGIC AND ROUTE LEVEL DELAY COMPOSITION ................................................................... 95
FIGURE 3-9 COMPONENT UTILIZATION IN INDIVIDUAL BLOCKS OF FIGURE 3-1 .......................................... 95
FIGURE 4-1 FLOW CHART FOR VEDIC DIVISION ALGORITHM – VEDIVISION ................................................ 124
FIGURE 4-2 PERFORMANCE ANALYSIS OF VEDIVISION VS NRD ALGORITHM ........................................... 127
FIGURE 4-3 QUOTIENT TIME ANALYSIS OF VEDIVISION AND NRD ALGORITHM ........................................ 128
FIGURE 4-4 HIGH LEVEL DIAGRAM FOR VEDIVISION HARDWARE ......................................................... 129
FIGURE 4-5 PERFORMANCE ANALYSIS OF COMPARISON FOR VEDIVISION AND NRD ON HARDWARE .... 133
FIGURE 4-6 PERFORMANCE ANALYSIS TAKING BCD TO BINARY AND BINARY TO BCD CONVERSION INTO
consideration ............................................................................................................................................. 135
FIGURE 4-7 GRAPHICAL SYNTHESIS TIME ANALYSIS FOR TABLE 4-11 ..................................................... 137
LIST OF TABLES

TABLE 1-1 THE 16 SUTRAS AND 13 COROLLARIES OF VEDIC MATHEMATICS WITH RESPECTIVE MEANINGS ..........4
TABLE 1-2 FOUR BIT WEIGHTED REPRESENTATION OF DECIMAL NUMBERS ......................................................... 6
TABLE 1-3 FOUR BIT CODED DECIMAL COEFFICIENT REPRESENTATIONS ...................................................................... 7
TABLE 1-4 MICROPROCESSOR FLOATING POINT UNIT COMPARISONS (SOURCE [113] [114] [115] [116]) .............15
TABLE 2-1 SINGLE DIGIT BCD ADDITION RESULTS WITH AN INCOMING CARRY .......................................................... 29
TABLE 2-2 REDUCED RESULT TABLE FOR CORRECTION FACTOR AND OUTGOING CARRY GENERATION ................. 30
TABLE 2-3 PATH DELAY FOR CONVENTIONAL SINGLE DIGIT BCD ADDER ............................................................. 38
TABLE 2-4 PATH DELAY FOR FAST SINGLE DIGIT BCD ADDER .................................................................................. 38
TABLE 2-5 PATH DELAY FOR 1:2 COMPRESSOR .............................................................................................................. 39
TABLE 2-6 PATH DELAY FOR COMPLETE 11 × 16 DIGITS BCD ADDER .................................................. 38
TABLE 2-7 PATH DELAY FOR SINGLE CORRECTION SPECULATIVE ADDER IN [50] FOR ADDING ELEVEN SINGLE DIGIT OPERANDS .............................................................................................................. 41
TABLE 2-8 PATH DELAY FOR WORD WIDE DECIMAL ADDER IN [50] ........................................................................ 42
TABLE 2-9 DELAY COMPARISON OF PROPOSED COMPLETE 11 × 16 DIGITS BCD ADDER OVER OTHER HARDWARE IMPLEMENTATIONS .................................................................................................. 43
TABLE 2-10 PERCENTAGE SPEEDUP OF PROPOSED COMPLETE 11 × 16 DIGITS BCD ADDER OVER SOFTWARE IMPLEMENTATIONS ........................................................................................................... 44
TABLE 2-11 TIME DELAY ANALYSIS FOR CONVENTIONAL BCD ADDER ............................................................. 45
TABLE 2-12 POWER AND TEMPERATURE ANALYSIS FOR CBA (OPERAND SIZE = 1 DIGIT) ........................................ 46
TABLE 2-13 POWER AND TEMPERATURE ANALYSIS FOR CBA (OPERAND SIZE = 2 DIGITS) ........................................ 47
TABLE 2-14 POWER AND TEMPERATURE ANALYSIS FOR CBA (OPERAND SIZE = 8 DIGITS) .................................... 48
TABLE 2-15 POWER AND TEMPERATURE ANALYSIS FOR CBA (OPERAND SIZE = 16 DIGITS) ........................... 49
TABLE 2-16 TIME DELAY ANALYSIS FOR PROPOSED FAST BCD ADDER ................................................................. 50
TABLE 2-17 POWER AND TEMPERATURE ANALYSIS FOR PFBA (OPERAND SIZE = 1 DIGIT) ............................................ 51
TABLE 2-18 POWER AND TEMPERATURE ANALYSIS FOR WWFBA (OPERAND SIZE = 2 DIGITS) .............................. 52
TABLE 2-19 POWER AND TEMPERATURE ANALYSIS FOR WWFBA (OPERAND SIZE = 8 DIGITS) ............................ 53
TABLE 2-20 POWER AND TEMPERATURE ANALYSIS FOR WWFBA (OPERAND SIZE = 16 DIGITS) .............................. 54
TABLE 2-21 THEORETICAL GATE DELAY AND PRACTICAL COMBINATIONAL PATH DELAY ANALYSIS ............. 55
TABLE 2-22 LOGIC DELAY ANALYSIS OF CONVENTIONAL VS PROPOSED FAST BCD ADDER ......................... 56
TABLE 2-23 ROUTE DELAY ANALYSIS OF CONVENTIONAL VS PROPOSED FAST BCD ADDER ............................ 56
TABLE 2-24 FPGA AREA UTILIZATION ANALYSIS ...................................................................................................... 57
TABLE 3-1 DIGIT-BY-DIGIT MULTIPLICATION USING NIHILAM SUTRA (CASE C4) ................................................. 64
TABLE 3-2 SIGNAL COMBINATIONS FOR REDUCED MAGNITUDE PARTIAL PRODUCT GENERATOR .................. 68
TABLE 3-3 TRUTH TABLE FOR ADDITION OF 0, 6 AND 12 ............................................................................................. 86
TABLE 3-4 DELAY CALCULATION FOR PARTIAL PRODUCT GENERATION IN [51]a ........................................................................ 88
TABLE 3-5 DELAY CALCULATION FOR PARTIAL PRODUCT GENERATION IN [62]a ............................................ 88

xv
Table 3-6 Delay calculation for partial product generation in [52]a ........................................ 89
Table 3-7 Delay calculation for partial product generation in [7]................................................ 90
Table 3-8 Performance analysis and critical path delay comparison for partial product reduction ................................................................. 91
Table 3-9 Critical path delay comparison for final addition .......................................................... 93
Table 3-10 FPGA synthesis results for reduced magnitude partial product generator ................. 94
Table 3-11 Power and temperature analysis for block 11 and block 14 (Figure 3-1).................... 96
Table 3-12 Power and temperature analysis for block 12 and block 15 (Figure 3-1)............... 97
Table 3-13 Power and temperature analysis for block 13 (Figure 3-1) ......................................... 98
Table 3-14 Power and temperature analysis for block 21 (Figure 3-1) .......................................... 99
Table 3-15 Power and temperature analysis for block 22 (Figure 3-1) ....................................... 100
Table 3-16 Power and temperature analysis for block 31 (Figure 3-1) ....................................... 101
Table 3-17 Power and temperature analysis for block 32 (Figure 3-1) ....................................... 102
Table 3-18 Power and temperature analysis for block 41 (Figure 3-1) ....................................... 103
Table 3-19 Power and temperature analysis for figure 3-1 ....................................................... 104
Table 4-1 Conversion table for divisor recoding ........................................................................... 116
Table 4-2 (8x4 cell) look up table / ROM for generation of quotient digit ............................... 117
Table 4-3 Look-Up Table for double digit dividend divisions (LUT2 / ROM2) ....................... 118
Table 4-4 Performance analysis – vedivision vs non restore type division algorithm .......... 126
Table 4-5 Data for quotient time analysis (selection from table 4-3) ..................................... 127
Table 4-6 Performance time comparison for vedivision and NRD on hardware ................. 133
Table 4-7 Extension of table 4-6 with BCD to binary and binary to BCD consideration ........ 134
Table 4-8 FPGA synthesis analysis for decimal division architectures ................................. 135
Table 4-9 CMOS cell implementation results for decimal division (precision: 16 digits) ........ 136
Table 4-10 Time analysis for major blocks in Figure 4-4 ....................................................... 137
Table 4-11 Component utilization summary for vedivision .................................................... 138
Table 4-12 Power and temperature analysis for vedivision hardware (Figure 4-4) .............. 139
Table 4-13 Power and temperature analysis for reduced magnitude divisor generator block (Figure 4-4) .................................................................................. 140
Table 4-14 Power and temperature analysis for vedic normalizer block (Figure 4-4) .......... 141
Table 4-15 Power and temperature analysis for vedic quotient placer block (Figure 4-4) .... 142
Table 4-16 Power and temperature analysis for further division decider block (Figure 4-4) .... 143
Table 4-17 Power and temperature analysis for quotient bank block (Figure 4-4) ............... 144
Table 4-18 Power and temperature analysis for ten’s complementing block (Figure 4-4) .... 145
Table 4-19 Power and temperature analysis for radix 10 vedic multiplier block (Figure 4-4) . 146
Table 4-20 Power and temperature analysis for LUT / ROM block (Figure 4-4) ................. 147