Conclusion

Chapter 5
CHAPTER 5

CONCLUSION

The envelope purpose of this thesis is to present digital designs for Radix 10 Arithmetic Processing. The author has proposed 6 novel designs encasing the four primitive decimal arithmetic operations, viz. Addition, Subtraction, Multiplication and Division on operands having a precision of 16 digits. The designs showcase Fixed Point Arithmetic and therefore can form the integral vital unit for Decimal Floating Point Arithmetic architectures attuned with IEEE decimal64 Decimal Floating Point specifications. The author believes that dedicated independent arithmetic units for processing the four primitive operations will definitely elevate processing speeds. The efficiency of the proposed designs have been judged on the parameters of Theoretical Logic Level Delay estimates as well as FPGA Synthesis estimations on Virtex5 / Spartan3E / Artix7 platforms. The FPGA implementations have remarkably supported the theoretical results. The author also admits that ASIC implementations will definitely be smarter than general purpose FPGA implementations, albeit both the hardware realizations reflect the theory. The next Subsection (Subsection 5.1) summarizes the proposed designs with Subsection 5.2 providing future research extension prospects of the work in this thesis.

5.1 SUMMARIZATION

This subsection summarizes the performance of the proposed decimal arithmetic designs in Chapter 2 through Chapter 4. The author has studied major literary contributions to decimal arithmetic hardware designs mentioned in Chapter 1 and focused on Ancient Vedic Sutras to design the two complex arithmetic operations, multiplication and division. All the proposed designs process BCD operands. Three of the sixteen Vedic Sutras have been engineered to design the Radix 10 Fixed Point Vedic Multiplier and Divider, each of the designs exploiting two sutras individually.

5.1.1 CHAPTER 2 – SUMMARY

The author has presented 4 decimal adder architectures processing BCD operands. The first of the four demonstrate a novel Single Digit Fast BCD Adder which lags behind the Conventional BCD Adder by mere three logic level delays, but when cascaded to add 16 digit operands, radically ousts the conventional counterpart. The cascaded design (Word Wide Fast BCD Adder) forms the second of the four proposals. The third design adds a column of 11 single digit BCD operands to generate a double BCD result, hence the name – 11:2 Compressor. The threshold of 11 single digit operands has been observed because if the operand count exceeds 11, then the result will be a triple BCD number or a double BCD number with an outgoing Carry wire. The final proposal, 11 × 16 Digit Radix 10 Fixed Point Adder, is capable of adding eleven 16 digit operands in parallel and exhibits better performance with
respect to a similar counterpart in literature. All the proposed designs excel over their literary counterparts both in terms of theoretical and synthesis delay estimates.

5.1.2 CHAPTER 3 – SUMMARY

This chapter engineers two Vedic Sutras, Nikhilam and Urdhva-Tiryakbhyam Sutra to design a Radix 10 Multiplier capable of multiplying two unsigned 16 digit operands. A Reduced Magnitude Partial Product Generator has been designed using the Nikhilam Sutra which executes single digit operand multiplication and generates valid double BCD result void of any correction. This design has been observed to excel over its literary counterparts in terms of both theoretical and FGPA synthesis analysis. Partial Product Accumulation has been done using the Urdhva-Tiryakbhyam Sutra. Partial Product Reduction and Final Carry Propagation Addition have been done using cascaded architectures of 3:2 Carry Save Adders and a novel Decimal Correction Unit. Four bit binary adders have been used for Final Carry Propagation Addition in combination with Speculative Correction Units for generation of valid BCD results. All the proposed designs excel over their counterparts in terms of the two judgment parameters.

5.1.3 CHAPTER 4 – SUMMARY

Nikhilam and the Paravartya Sutras are the two Vedic Sutras employed for designing the Radix 10 Fixed Point Divider in this chapter. Operational limitations imposed by both the sutras compelled the author to design a generic algorithm (Vedivision) based to process any pair of operands. After successful software implementation of Vedivision and observing better performance time with respect to a software version of the Non Restore Type Division Algorithm, the author implemented the algorithm on hardware using FPGAs.

5.2 RESEARCH EXTENSION PROSPECTS

This thesis has presented architecture designs for Decimal Fixed Point Arithmetic. The present work can be research extended in floating point domain. BCD Vector processors and important mathematical function architectures, viz. Exponentials, Logarithms etc, can be a potential area of further research. Cryptography being a division intensive domain, Decimal Crypto-Processors with inbuilt Division and Modulus architectures can enable High-Speed Cryptography. Financial computers based on dedicated binary and decimal processors with binary addressing modes can be a short call with extended research in mixed radix architectures, primarily binary and decimal. The author has used three of the sixteen Vedic sutras. The rest thirteen Vedic Sutras and thirteen corollaries can be further investigated to design high speed decimal application oriented accelerators.