Chapter - 1

INTRODUCTION

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1.1 Overview

By the turn of the twentieth century, the Integrated Circuit (IC) has led a revolution in all spheres of life ranging from communication, industrial automation, military and other disciplines. ICsare made of tiny,discreet Metal-Oxide-Semiconductor structures or MOS devices, where single crystal silicon is used as a substrate. To enhance the speed, reliabilityand performance of ICs,thesize of the MOS structure is scaleddown and the largestpossible number of MOS is etched into theleast possible area on a substrate called the chip. Presently, billions of MOS devices are routinely integrated together in a small chip. The scaling down of MOS deviceson a silicon substrate has reached its limit at the nano-meter scale and further scaling down is not possible. For future advances one alternative is to develop nano-materials that can substitute silicon. While commercial development of nano-material-based ICs may take a few more years, prototypeICshave already been developed. Another alternative is to develop devices with other materials which have higher carrier mobility than silicon. This approach does not need further scaling down of MOS structuresand also givesflexibility in IC design and fabrication. In addition, ICs or devices made with these new materials will open up new areas of applications.

The materials that are mostly used in the field of electronics are metals, semiconductors or insulators. All the three materials basically differ in terms of their band-gap energy. For metals the band-gap is 0V, whereas for insulators it is quite large, about 5eV or more. The band-gap of semiconductors lie in-between these two materials-neither as high as insulators nor as low as metals. The fundamental issues in this field involves the knowledge, not only on different types of materials, but also of the structural and electrical properties of materials like crystal structure, planes, defects, impurities, surfaces, interfaces, conductivity, resistivity, doping etc. Amongst all of these properties the concept of surface and interface has gained special importance in the case of solid-state physics. Surfaces and interfaces are cross-disciplinary fields of science and technology, thus gaining importance in the advanced technology of today, particularly in modern electronics. A surface or interface is a common boundary between two different phases of matters. Although the two

words are often used synonymously, the latter term is preferred for the boundary between two explicitly named phases. A number of permutations are possible in the formation of an interface such as solid-solid, solid-liquid, liquid-gas, solid-gas etc. Knowing the quality of the interface formed is of great importance for understanding the different behavioural aspects of both the interface and the bulk material. By knowing the properties of interfaces, the characteristics of the electronic devices made out of different materials can be better understood.

Thus, present-day electronics requires even better understanding and control of interfaces to achieve the desired electrical characteristics of devices. This is because the interaction of different materials at their boundaries depends on the physical and chemical conditions of the interfaces. As the next generation of electronic devices progressively reduce insize towards the nanoscale region, interactionsbetween different materials get increasingly dominated by surfaces and interfaces. Thus, the analysis of surfaces and interfaces is imperative to study prior to attempts to fabricate devices with these materials.

In this thesis,different properties are studied for the bulk and thin films of the semiconductor, Gallium Antimonide (GaSb),of the High-K dielectrics, Zinc Oxide (ZnO), Aluminum Oxide (Al_2O_3),Hafnium Oxide (HfO_2)and of Indium Arsenide (InAs)which is used as a passivating agentin between the semiconductor and oxide interfaces, as materials in different types of devices like the Schottkydiode, the heterojunction diode and the MOS capacitor,based on different types of interfaces.

1.2 Basic Classification of Interfaces

The understanding of interfaces depends on the different classes of materials involved, like metals, semiconductors and insulators. However, the interfaces of importance in electronic applications are metal-metal, metal-semiconductor, semiconductor-semiconductor, and semiconductor-insulator interfaces. Basically, out of these,three types of interfaces can exist with semiconductor material— interfaces with conductors, interfaces between two different semiconductors and interfaces with insulators. In this sectionthese three types of interfaces shall be briefly discussed.

1.2.1 Semiconductor-Metal Interface

The behaviour of the interface between a metal and a semiconductor is an importantaspect in semiconductor devices. To understand the physical behaviour at this interface, the charge density of both electrons and holes need to be considered. This is because, generally in semiconductors, the majority carriers are considered, but in the case of conductors usually the minority carriers are considered for the surface combination. Such considerations are appropriate for conductors since the relative change in carrier densities is due to recombination at the interface which largely affectsthe life time of minority carriers but is negligible for majority carriers.

At the metal-semiconductor interface a potential barrier exists between the two materials preventing the passage of charge carriers from one to another. Only a small number of carriers acquire sufficient energy to cross the barrier to reach the other material. Two effects can be seen on the application of an external bias—either the barrier potential may increase or decrease when viewed from the semiconductor side. The bias does not change the barrier height from the metal side. The details in the variations of potential barriers between the metal and the semiconductor under no-bias condition can be identified on an energy band diagram where,

$E_c$andE_v = Conduction band edge energy and valence band edge energy level.

E_{vac}andE_F = Energy of Vacuum level and Fermi energy level

ϕ_s = Work function of the semiconductor, the energy required to bring an electron from the Fermi level to the vacuum level

$= \frac{E_{vac}-E_f}{q}$, therefore $\phi_s$depends on the doping level of the semiconductor.

χ = Electron Affinity, the energy required to bring an electron from the conduction band to the vacuum level.

$= \frac{E_{vac}-E_c}{q}$, a property of the material, independent of doping concentration.

$\Phi_{ms} = \phi_m - \phi_s$ = metal-semiconductor work function difference.

If $\phi_m > \phi_s$, the total energy of the metal/semiconductor system reduces due to the flow of electrons from the semiconductor to the metal side to establish equilibrium by maintaining E_F constant.

Using these guidelines, the band diagram of a metal-semiconductor interface can be drawn as shown in Figure 1.1

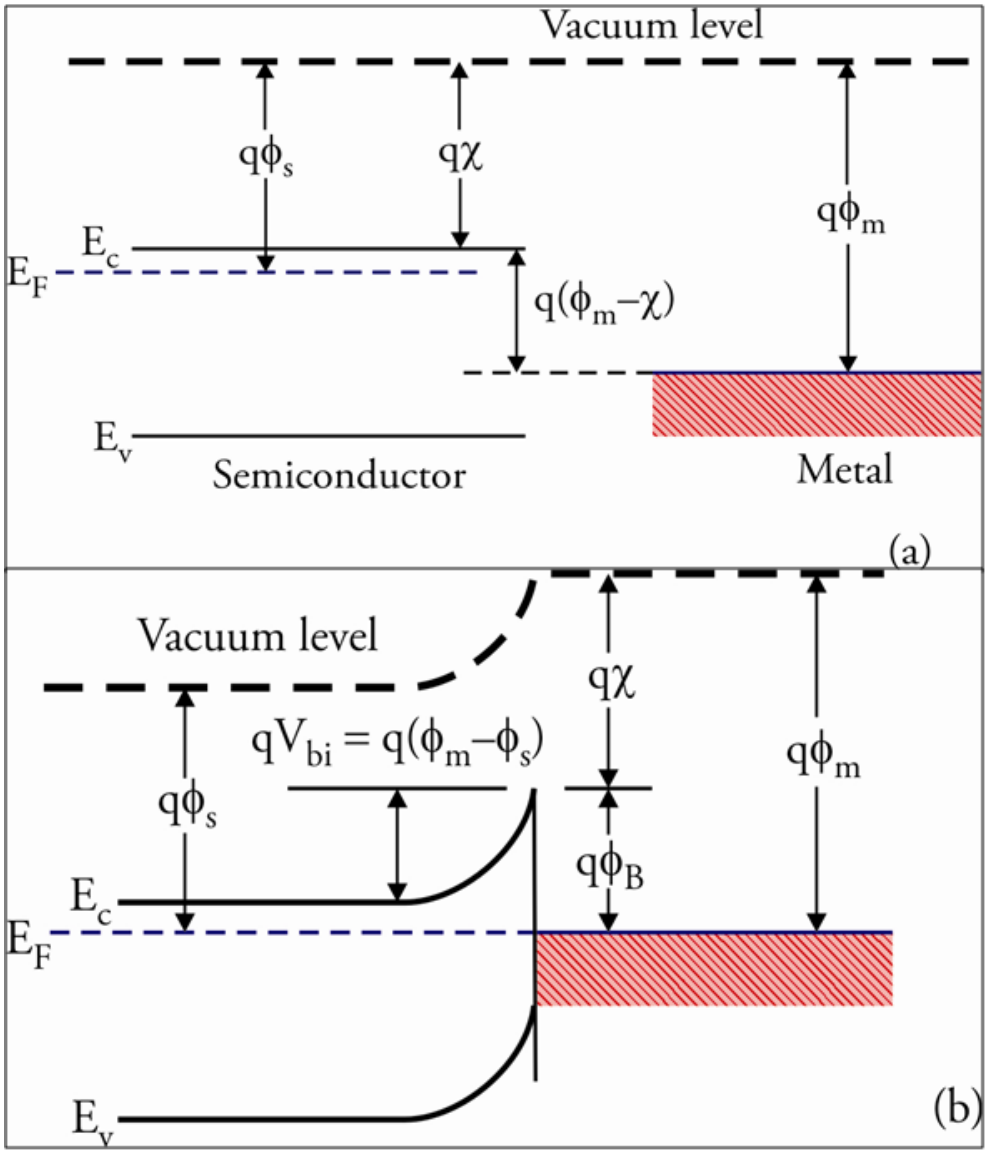

Figure 1.1. Energy Band Diagram of (a) Metal Adjacent to a Semiconductor underThermalNon-equilibriumConditions, (b) Metal-Semiconductor Contact in Thermal Equilibrium

The electrical characterisation of a metal-semiconductor interface and its quality is determined by interface properties like barrier height (ϕ_B) and ideality factor (η). Inan ideal case,where the ideality factor is usually taken as 1,thebarrier height is simply the difference between the metal work function and the electron affinity of the semiconductor. Inpractice,

these performance parameters can be computed from the forward-bias current transport mechanism of the metal-semiconductor interface, which obeys the thermionic emission principle [1-3]. When voltage (V) more than 3KT/q is applied, then the thermionic current can be calculated by the formula,

$$I = I_0 \exp\left(\frac{qV}{\eta kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (1.1)$$

Where I_0 is the reverse saturation current density, which can be defined as

$$I_0 = A^{**}T^2 \exp\left(-\frac{q\,\phi_B}{kT}\right) \quad (1.2)$$

Where A^{**} is the effective Richardson constant and Φ_B is the barrier height of the metal-semiconductor interface, and η is theideality factor and calculated as:

$$\eta = \left(\frac{q}{KT}\right)\frac{d(V)}{d(lnI)} \quad (1.3)$$

Using equation 1.3, if ln I is plotted againstthe forward voltage,the intercept at Y-axis gives the reverse saturation current I_0 and the slope of the plot can be used to obtain theideality factor (η). In addition to this, the barrier height (Φ_B) can also be determined from equation 1.2.

Besides this, another technique, called the high frequency (1MHz) capacitance-voltage characteristics (C-V),can be used to determine the barrier height (Φ_B) of the diode using equation 1.4 and the plot drawn between voltages versus inverse of C^2 as shown in Figure 1.2.

$$\phi_B = V_{diff} + \phi_{fn} + \frac{KT}{q} \quad (1.4)$$

Where V_{diff}can be determined from the voltage versus inverse of C^2 plot from the data of C-V characteristic, Φ_{fn} is the potential difference between the Fermi level and the conduction band edge, K the Boltzman's constant, T is the temperature and q is charge of an electron.

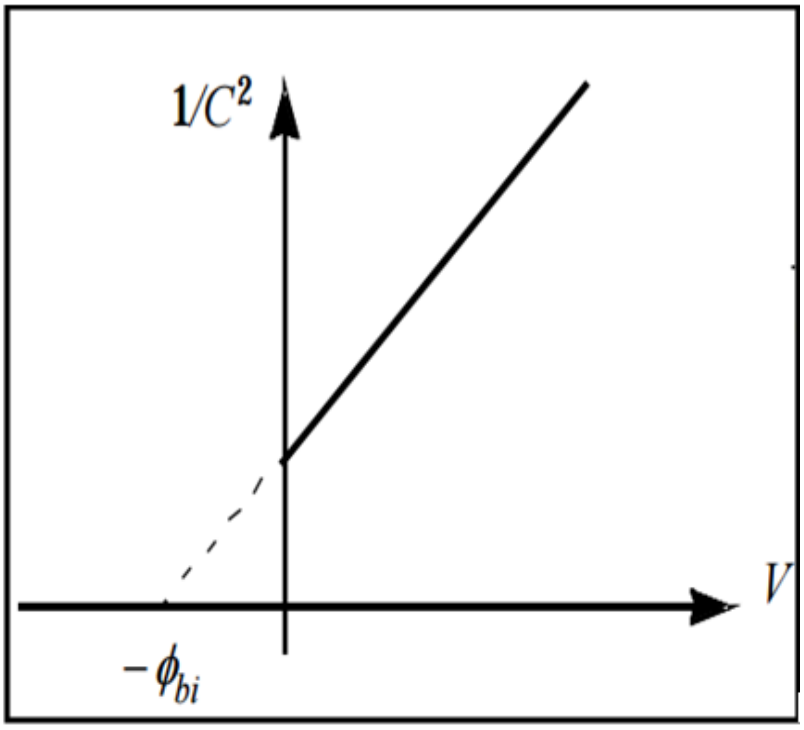

Figure 1.2 Plot of Voltage v/sInverse of C^2

Metal-semiconductor interfaces, also known as Schottky diodes orSchottky barrier diodes,were widely used for RF applications like mixers or detector diodes for theirhigh switching speeds and high frequency capabilities. These diodesarealso used in power applications as rectifiers due to theirlow turn-on voltage and high current density that result in low power dissipation as compared toordinary diodes. Besides this,Schottky diodesarealso used inpower OR circuits, solar cell applications, clamp diodes etc.

1.2.2 Semiconductor-Semiconductor Interface

Atthe interface between two types of semiconductors, materialsdiffuse into each other and form a junction. More specifically, a *pn*- junction diode is formed when a *p*-type doped portion of a semiconductor is in contact with the *n*-type doped portion or vice versa. If both the *p*-type and *n*-type regions are of same type of semiconductor material, then the junction is called a homojunction. If the junction layer at the interface is formed between two different semiconductors then it is called a heterojunction.

In aheterojunction, these two different types ofsemiconductor materials have different band-gaps. During the formation of a heterojunction, three possible situations may

arise during the alignment of the band gap energies, as is shown in Figure 1.3. In one case, called straddling (Type 1), the forbidden band-gap of the wide-gap material completely overlapsthe band gap of the narrow gap material. The other possibilities are called staggered gap (Type-II), and broken gap (Type-III).

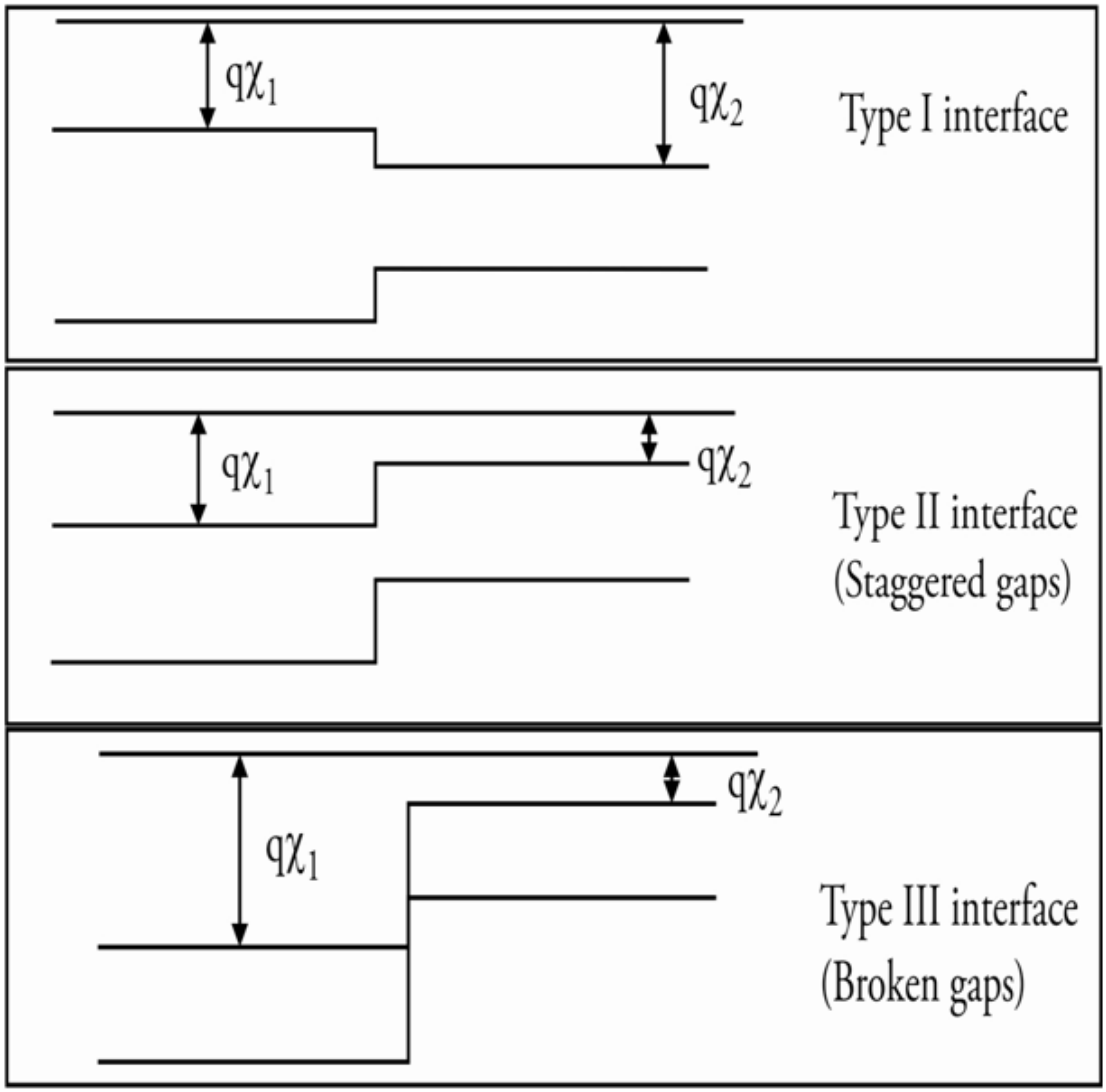

Figure 1.3: Band Alignments Causing Different Types of Heterojunctions

Electricalproperties of the heterojunction are dependent on the alignment of the energy bands at the interface of the twosemiconductors. To predict the energy band alignment, different models have been proposed:

Anderson's Model

Thisis the simplest among all themodels. This rule predicts the 'band alignment'of vacuum-semiconductor interfaces. It is also referred to as the electron affinity rule and is closely related to Schottky-Mott rule for metal-semiconductor junctions [3].

Common-Anion Rule

This rule was proposed based on aguess related to the anionic state of the valence band. This explains that materials having the same anions have very small valence band offset, whereas two materials with different anions have larger valence band offset as compared tothe conduction band offset [4].

Gap State Model

This model has been proposed by Tersoff based on the metal-semiconductor interface. This model incorporates a dipole layer arising due to the electron tunnelling from the conduction band of one material into the band gap of the other material at the interface between the two semiconductors. The only limitation ofthis model is that it agrees well with experimental data only for semiconductor materials like GaAs and AlGaAsthat havelattices that closely match with each other [4].

60:40 Rule

This is a heuristic approach for specific cases like GaAs and its alloys. For example, in case of $Al_xGa_{1-x}As$, as x varies from 0 to 1 the ratio of $\Delta E_C/\Delta E_V$ remains approximately at 60/40. This has been compared for its correctness with a GaAs/AlAs junction which has a ratio of $\Delta E_C/\Delta E_V$= 0.73/0.27 [5].

When two different semiconductors are brought into contact, the electrons tend to flow from the region with higher Fermi level (*n*-region) to the region with lower Fermi level (*p*-region) or holes flow from the lower Fermi level (*p*-region) to the higher Fermi level (*n*-region). As these mobile charges move towards the other sides, they leave behind uncompensated parent ions. In the *n*-region the uncompensated ions are positive ions and vice versa. This carrier diffusion results in an electric field pointing from the *n*-region to the *p*-region. This electric field retards both the electron and hole diffusion from *n*-side to *p*-side and vice versa. Hence, a natural negative feedback mechanism works such that the

more a carrier movement takes place the more the electric field strength increases. The larger the electric field becomes; the movement of carrier reduces gradually to such an extent that an equilibrium condition is establishedbetween the carrier diffusion and the electric field as a result of the alignment of the fermi levels of the two regions. The dopants from both sides that became uncompensated during this instantaneous exchange process form a region called the depletion region or space-charge region. The regions beyond the depletion region remain similar to that of bulk material, still compensated by their respective electrons or holes. These are called the neutral regions, where the net charge concentration is zero. Thus, the band discontinuities and the band bending at the junction can be drawn accurately for a heterojunction. The approximate band diagram can be sketched by solving Poisson's equation considering the doping and space charge [1-3].

LetX=0 corresponds to the junction boundary and then*n*-side be in the positivex-direction and the *p*-side be in the negative x-direction. Furthermore, we define $X=X_{N0}$to bethe boundary separating the depletion and neutral regions on the *n*-side and $X=X_{p0}$ to be the boundary on the *p*-side. Then, under thermal equilibrium conditions, the solution of Poisson's equation can be used to establish the band edges of the conduction and valence bands across the depletion region using the following equation:

$$\frac{d\varepsilon}{dx} = \frac{q}{\epsilon_s}(p - n + N_d - N_a) \tag{1.5}$$

As it is known that, in the *n*-side depletion region the net charge density is due to the donors and in the *p*-side depletion region the net charge density is due to the acceptors. Therefore, the equation 1.5 can be simplified to

$$\frac{d\varepsilon}{dx} = \frac{q}{\epsilon_N}N_d \quad for \quad 0 < x < x_{N0} \tag{1.6}$$

$$\frac{d\varepsilon}{dx} = -\frac{q}{\epsilon_p}N_a \quad for \; -x_{p0} < x < 0 \tag{1.7}$$

On integrating and applying the boundary conditions that the electric fields at x_{N0} and at $-x_{p0}$ are zero, the electric field within the depletion region can be found by the equations:

$$\varepsilon_x = -\frac{q}{\epsilon_N}N_d(x_{N0} - x) \quad for\, 0 < x < x_{N0} \tag{1.8}$$

$$\varepsilon_x = -\frac{q}{\epsilon_p}N_a(x + x_{p0}) \quad for -x_{p0} < x < 0 \tag{1.9}$$

On the *n*-side, the relative potential profile, rather than their absolute values,isobtained by integrating ε(x)

$$V(x) = -\int \varepsilon_x \, dx = \frac{q}{\epsilon_N} N_d \left(x \, x_{N0} - \frac{x^2}{2} - \frac{x_{N0}^2}{2} \right) \quad for \; 0 < x < x_{N0} \tag{1.10}$$

The built-in potential on the *n*-side (ϕ_{n0}) is the difference in the potentials at x=0 and $x=x_{n0}$.

$$\phi_{N0} = \frac{q}{2\epsilon_N} N_d x_{N0}^2 \tag{1.11}$$

Similarly, the potential profile and the built-in-potential on the *p*-side can also be obtained by integrating the appropriate electric profile and from the difference in potentials at x=0 and $x= -x_{p0}$ respectively.

$$V(x) = -\int \varepsilon_x \, dx = \frac{q}{\epsilon_p} N_a \left(x \, x_{p0} + \frac{x^2}{2} + \frac{x_{p0}^2}{2} \right) \quad for \; -x_{p0} < x < 0 \tag{1.12}$$

$$\phi_{p0} = \frac{q}{2\epsilon_p} N_a x_{p0}^2 \tag{1.13}$$

The overall built-in potential (V_{bi}) is the potential difference between the two neutral regions present on either side of the junction. It is equal to

$$V_{bi} = \phi_{N0} + \phi_{p0} = \frac{q}{2\epsilon_N} x_{N0}^2 + \frac{q}{2\epsilon_p} x_{p0}^2 \tag{1.14}$$

$x_{N0}$and x_{p0}can be determined by solving two linearly independent equations relating these two variables. The first equation can be obtained by using Gauss' theorem, which explains the continuity of the electric flux density D=Єε in the absence of an interfacial charge density at the junction,

$$N_d x_{N0} = N_a x_{p0} \tag{1.15}$$

The expression defines the charge neutrality condition existing all over the *pn*-junction. Thus, the second linear equation used to determine the value of x_{N0} and x_{p0} is the ratio of the built-in potentials on the n-side to those on the p-side,

$$\frac{\phi_{N0}}{\phi_{p0}} = \frac{\epsilon_p \; N_d x_{N0}^2}{\epsilon_N \; N_a x_{p0}^2} \tag{1.16}$$

Substituting the equation 1.11 in equation 1.12, the ratio can be rewritten as

$$\frac{\phi_{N0}}{\phi_{p0}} = \frac{\epsilon_p\ N_d}{\epsilon_N\ N_a} \tag{1.17}$$

From the above equation, the built-in potential of the junction is

$$V_{bi} = \left(1 + \frac{\phi_{N0}}{\phi_{p0}}\right)\phi_{p0} = \left(1 + \frac{\epsilon_p\ N_d}{\epsilon_N\ N_a}\right)\phi_{p0} \tag{1.18}$$

As per the depletion approximation, majority carrier concentration is zero at the depletion regions x= x_N and x= $x_p$on the n-side and p-side respectively. Thus, using the equation 1.11 the X_n and X_p can be found out as,

$$x_n = \sqrt{\left[\frac{2}{q}\varepsilon_p\varepsilon_N\frac{N_a}{N_d}\frac{V_{bi}}{(\varepsilon_p N_a+\varepsilon_N N_d)}\right]} \tag{1.19}$$

$$x_p = \sqrt{\left[\frac{2}{q}\varepsilon_p\varepsilon_N\frac{N_d}{N_a}\frac{V_{bi}}{(\varepsilon_p N_a+\varepsilon_N N_d)}\right]} \tag{1.20}$$

Therefore, the total depletion thickness is found to be,

$$W = x_n + x_p = \sqrt{\left[\frac{2}{q}\frac{\varepsilon_p\varepsilon_N}{(\varepsilon_p N_a+\varepsilon_N N_d)}\frac{(N_a+N_d)^2}{N_a N_d}V_{bi}\right]} \tag{1.21}$$

Charge per unit area on one side of the junction is given by $N_d x_{N0} = N_a x_{p0} = 0$

$$Q = \sqrt{2q\frac{\varepsilon_p\varepsilon_N N_a N_d}{(\varepsilon_p N_a+\varepsilon_N N_d)}V_{bi}} \tag{1.22}$$

Also, from the band diagram the built-in-potential can be calculated by using the following equation,

$$V_{bi} = \frac{E_{gp}+\Delta E_c-\phi_p-\phi_N}{q} \tag{1.23}$$

Where $E_{gp}$is the energy gap of the p-side material, ϕ_N and ϕ_p are the differences of the Fermi levels with respect to the conduction band edge and valence band edge respectively. Once doping levels for both the *p*- and *n*-regions are defined then ϕ_p and ϕ_N can be calculated and finally V_{bi} can also be calculated. Other quantities such as ϕ_{N0}, ϕ_{p0} and V(x) are then obtained fromthe equations derived above.

1.2.3 Oxide-Semiconductor Interface

The metal-oxide-semiconductor interface or MOS capacitor (MOSCAP)can be found in most semiconductor devices and is thus an important structure. In large scale integrated circuits, Metal Oxide Field Effect Transistors (MOSFETs) areimportant components in which MOSCAPsare an essential part. Therefore, all the studies related to any kind of MOS device needs the understanding of the MOS structure first. The MOS capacitor consists of an oxide film sandwiched between a *p*- or *n*-type semiconductor substrate and a metal plate called a gate.

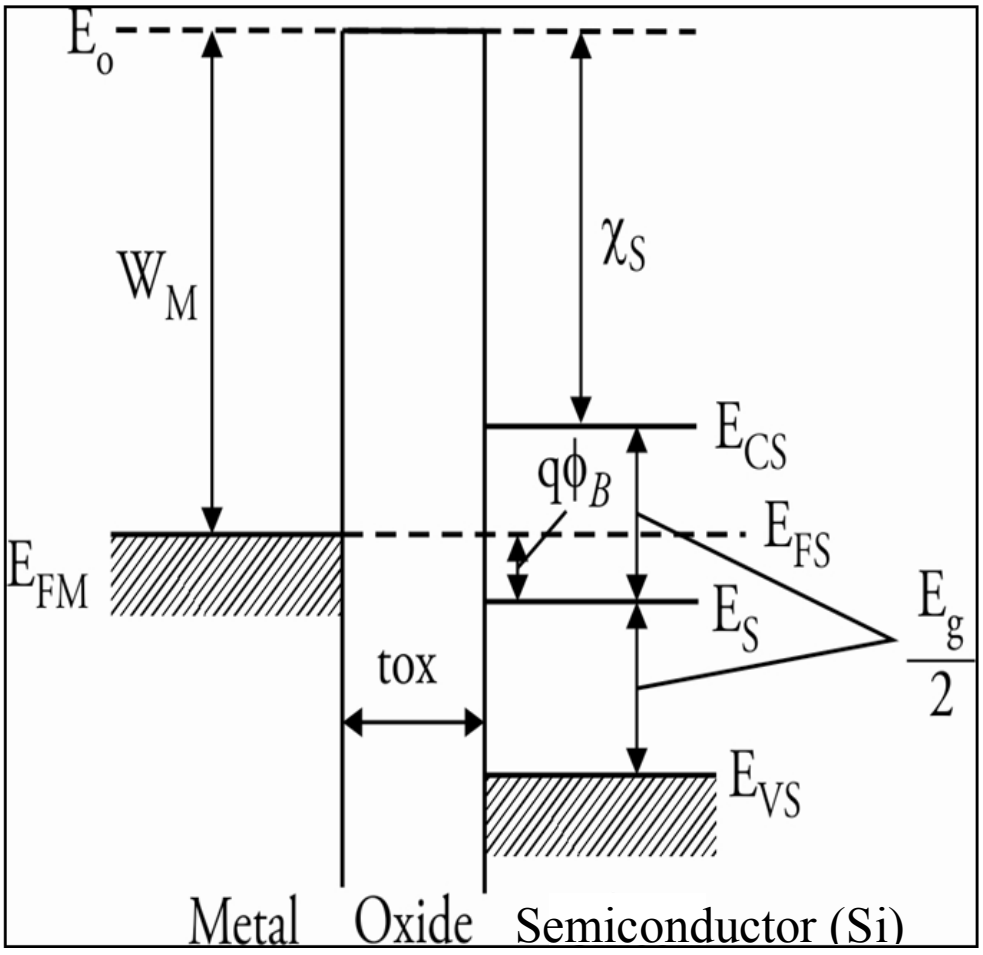

Figure 1.4: Energy Band Diagram of Unbiased Ideal MOS Structure

Before characterising the electrical properties of real MOS structures, an ideal MOS structure, which makes for a simple electrical analysis, is considered. The MOS structure is called ideal when the following two conditions are met: First of all, the metal work function

W_M and semiconductor work function W_S must be equal (i.e. $W_M = W_S$) in other words, all energy levels are flat when no voltage is applied to the MOS structure. This case is illustrated in Figure.1.4, where silicon is considered as semiconductor. In addition, there should be no chargesare present either in the oxide or at the semiconductor-oxide interface, which implies that in the absence of any applied voltage, the electric field is zero everywhere.

The oxide-semiconductor interface can be properlyunderstood when the Capacitance-Voltage (C-V) characteristics of a MOSCAP structureare studied as a function of the frequency. The C-V measurement is a powerful and commonly used method for determining interface properties like gate-oxide thickness, substrate-doping concentration, threshold voltage, flat-band voltage, interface-trap density etc. [1-3]. Adetailed study of the C-V characteristics of a MOSCAP can be divided into three distinct regions; Accumulation region, Depletion region and Inversion region as shown in Figure 1.5. In the accumulation region, the MOSCAP is just a capacitor with maximum capacitance C_{ox}. In the depletion region, the MOSCAP consists of two capacitors in series—the oxide layer capacitor (C_{ox}) and the depletion layer capacitor (C_{dep}). Under asmall AC signal voltage, the depletion width (W_{dep}) expands and contracts slightly in response to the AC frequency. Therefore, the AC charge appears at the bottom of the depletion layer and W_{dep}varies as a function of V_g. As V_g increases beyond the flat-band voltage (V_{fb}), W_{dep} expands, and the overall capacitance decreases. In the inversion region, in response to the AC signal, Q_{inv} follows the AC frequency. The inversion layer plays the role of the bottom electrode of the capacitor. Therefore, the capacitance reverts to C_{ox} after the inversion region in case of a low frequency signal, whereas, in case of a high frequency response the C-V characteristic cannot revert back to C_{ox} after the inversion. Thus one can distinguish between low frequency C-V characteristics from that of high frequency C-V characteristics. Thus, C_{HF} is represented as high frequency capacitance while C_{QS} as quasi-static and low frequency capacitance [1-3].

The two voltages that demarcate the three regions are (a) Flat-band Voltage (V_{FB}) and (b) Threshold Voltage (V_T). Flat-band voltage separates the accumulation region from the depletion region and threshold voltage separates the depletion region from the inversion region.

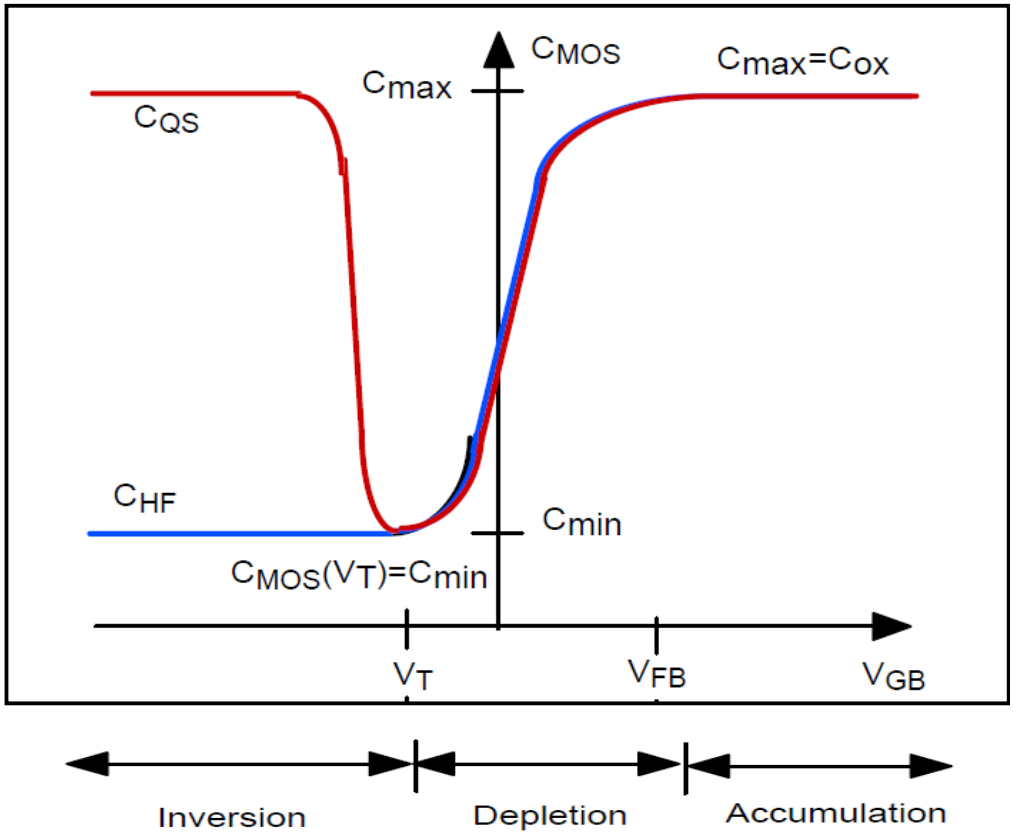

Figure 1.5. C-V Diagram of aMOSCAP [2].

In theory, the flat-band voltage is defined as the applied gate voltage when there is no band bending in the semiconductor, and as a result the net space charge in this region is zero.

$$V_{FB} = -\phi_B = -(\phi_M - \phi_s) \tag{1.24}$$

Where, φ_M = Work-function of metal and $\phi_s = \chi - \frac{E_g}{2} + \phi_{Fp}$ (1.25)

In real devices, there is a positive charge located at the oxide/semiconductor interface and it modifies the equation as follows

$$V_{FB} = -(\phi_M - \phi_s) - Q_i\left(\frac{t_{ox}}{E_{ox}}\right) \tag{1.26}$$

Where, Q_i = Interface Charge Density at Oxide/Semiconductor interface.

Whereas, the threshold voltage in case of a general MOS systems is defined as the applied gate voltage required achieving the threshold inversion point. The threshold inversion point, in turn is defined as the condition when the surface potential is $\varphi_S = 2\varphi_{fp}$for

the p-type semiconductor and $\varphi_S = 2\varphi_{fn}$ for the n-type semiconductor. Threshold voltage is given by the equation,

$$V_T = V_{FB} - 2\phi_n - \frac{t_{ox}}{E_{ox}}\sqrt{2\epsilon_s q N_D(2\phi_n)} \quad (1.27)$$

Where V_{FB} is the flat-band voltage, N_i is the intrinsic concentration, T_{ox} is the oxide thickness, $N_d$is the substrate doping, $E_{ox}$and E_s are the dielectric constants of oxide and substrate.

During the fabrication of the MOS device, different kinds of defects get introduced at the oxide-semiconductor interface. Interface trapped charge, also known as interface state is one of the defects which generally resides at the oxide-semiconductor interface. These trapped charges are due to structural imperfections or dangling bonds. Interface traps are a continuum of energy levels and are quantified as interface trap density (D_{it}). Interface traps are electrically active and situated within the band-gap. These charges also exist within the conduction & valence bands but are indistinguishable from the large density of band states. D_{it} acts as a generation/recombination centre and contributes to current leakage, low-frequency noise, reduced mobility, drain current, and trans-conductance and is expressed by the following formula:

$$D_{it} = \frac{Ci}{q}\left[\left(\frac{d\psi s}{dV}\right)^{-1} - 1\right] - \frac{Cd}{q} \quad (1.28)$$

Where, C_i is insulating capacitance, C_d the depletion capacitance and $\psi_s$is the surface potential.

1.3 Material Systems for Interface Studies

The interface properties that decide the kind of charge transport takesplace between twomaterials depend on two basic factors. One of them is the constituent materials that form the junction and the other one is the condition under which the junction is formed. Thus, an enormous range of physical propertiescan be created by combining different types of materials,constrained factors like the geometrical, chemical, physical, and electrical properties of the materials.Thus, thefirst aspect that needs to be studied is the selection of the semiconductor materials for the fabrication of a particular device. Semiconductors are elements inthe periodic table thatoccupy aposition intermediate betweenmetals and non-metals. The elemental semiconductors like silicon and germanium are located in group IV.

Even though the use of germanium as a semiconductor was discovered first, today, silicon dominatesthe field of electronicsand is expected toremain so for the foreseeable future. Apart from elemental semiconductors, compound semiconductors are also commercially available. Today the most commercially significant compound semiconductors are Gallium Arsenide (GaAs), Indium Phosphide (InP), Gallium Nitride (GaN), Indium antimonide (InSb), Aluminum Arsenide (AlAs) etc. which are examples of III-V compound semiconductor. From the time of the discovery of III-V compound semiconductors;there has been a lot of interest in these materials as most of them are direct band-gap and high mobility materials. Thus, they have turned out to be the obvious choice in the field of photonic devices and high-speed electronics. Their importance in applicationslike light emitting diodes (LED), lasers, photo-detectors, high electron mobility transistors (HEMT) were soon recognised after their discovery. Among compound III-V semiconductors, gallium antimonide (GaSb) and GaSb-based devices are promising candidates for a variety of military and civilian applications. As a matter of fact, this material has proved to bea suitable candidate for both basic and applied research. We have, therefore, chosen to work on these materials. Before proceeding further,it is important to briefly describe the relevant structure and properties of some of the materials used in this thesis.

1.3.1 Gallium Antimonide (GaSb)

Out of the III-V compound semiconductors,Gallium Antimonide (GaSb) has received special attraction due to its properties that make it suitable for advanced electronics devices, like a lattice constant of 6.095 Å, a direct band gap of 0.72eV, electron mobility of $\leq$ 4000 $cm^2V^{-1}s^{-1}$, high hole mobility ($\leq$ 1400 $cm^2V^{-1}s^{-1}$). Irrespective of growth conditions undopedGaSb is always *p*-type in nature. It also has a Zinc blende crystal structure [6-13]. Although the zinc blende structure is closely related to the diamond structure but the diamond lattice has a centre of inversion midway between two atoms in primitive cell, whereas the zinc blende lattice does not posse this property. Figure 1.6 shows the crystalline structure of GaSbconstituting two Face Centred Cubic (FCC) sublattices formed by the atoms Ga and Sb where one Ga atom remains tetrahedrally surrounded by four Sb atoms and vice versa. The bonding forces in such semiconductor compounds are partially covalent and partially ionic. Crystals lacking centres of inversion can be strongly nonlinear, and that leads to nonlinear optical properties that are shown by GaSb [6-13]. Thus, in the field of modern electronic devices, GaSb is particularly suitable

for fabricating optoelectronic devices in the range of 0.3eV (InGaAsSb) to 1.58eV (AlGaAsSb) as a substrate material. It is also an ideal candidate for thermo-photovoltaic (TPV) application with radiation temperature close to 1100^{o}C. Formation of quantum wells in type II InAs/Ga(In)Sb superlattices material systems make it suitable for application, in the Infrared range of 3 μm to 30 μm, as detectors, lasers and modulators. Thus,GaSb has proved itself as an ideal material for the study of Augur recombination process due to its band structure [6, 15].

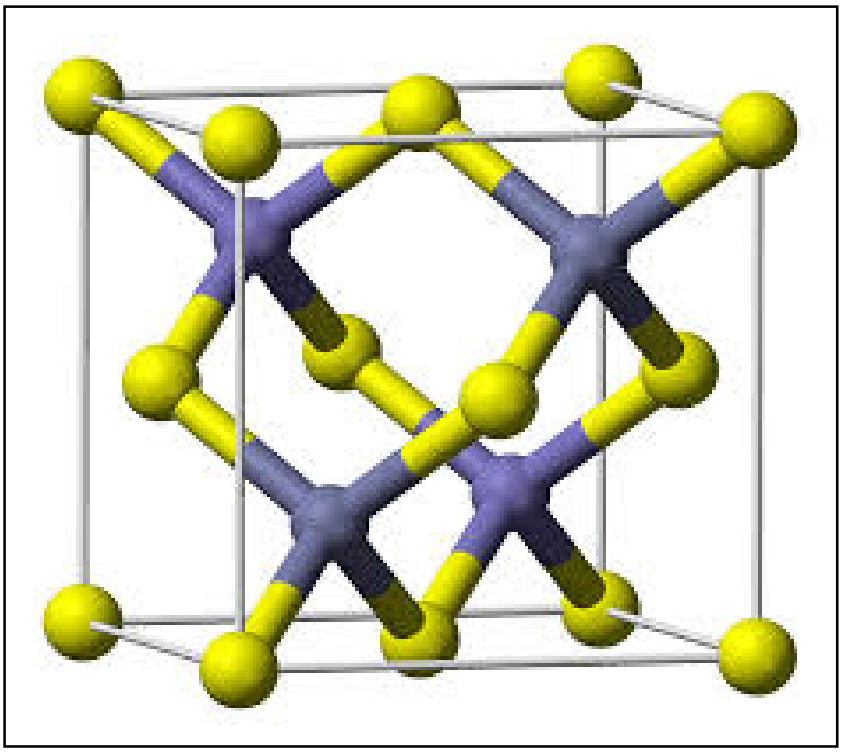

Figure 1.6. Zinc blende structure of GaSb, Yellow and BlueSpheres Denote Ga and SbAtoms, Respectively [14]

However, the major problem associated with the use of GaSb in the area of electronics is its high substrate cost, which is mainly due to its high processing cost. Besides the cost, the GaSb surface is highly reactive to oxygen and forms GaO_x and SbO_x when exposed to air. Furthermore, SbO_x, being thermally unstable, reacts with the GaSb substrate to form Ga_2O_3 and elemental Sb. Formation of elemental Sb causes the formation of a GaSb surface prone to current leakages, which is a major roadblock in the use GaSb as a substrate material [6, 15].To overcome the limitations of GaSb, researcher has given much more attention on oxide-based semiconductors like ZnO, Al_2O_3, SnO_2, HfO_2 etc. Out of these, ZnO has attracted a lot of attention for optical applicationsdue to high activation

energy of 60meV and wide bandgap of 3.37eV.A few more physical properties of GaSb are listed in table 1.1.

Table 1.1: A Few Physical and Electrical Properties of GaSb[6-13]

Properties	Values
Crystal Structure	Zinc Blende
Cleavage plane	<110>
Lattice Constant	6.095 Å
Band Gap	0.72 eV (Direct Type)
Intrinsic Carrier Concentration	1.5×10^{12} cm^{-3}
Electron Mobility	≤ 4000 cm^2 V^{-1} s^{-1}
Hole Mobility	≤ 1400 cm^2 V^{-1} s^{-1}
Melting Point	712 °C
Thermal Conductivity	0.32 W cm^{-1} $°C^{-1}$
Bulk Modulus	5.63×10^{11} dyne cm^{-2}
Density of the crystal	5.61 $g.cm^{-3}$
Debye temperature	266^0 K
Refractive Index	5.165
Dielectric constant	15.7
Electron affinity	4.06
Work function	4.76 eV
Effective density of states in the conduction band, N_c	1.76×10^{18} cm^{-3}
Effective density of states in the valence band, N_v	8.87×10^{18} cm^{-3}
Effective mass of electron, m_e	$0.041m_0$
Effective mass of hole, m_h	$0.4m_0$

1.3.2 Zinc Oxide (ZnO) and High-K Materials

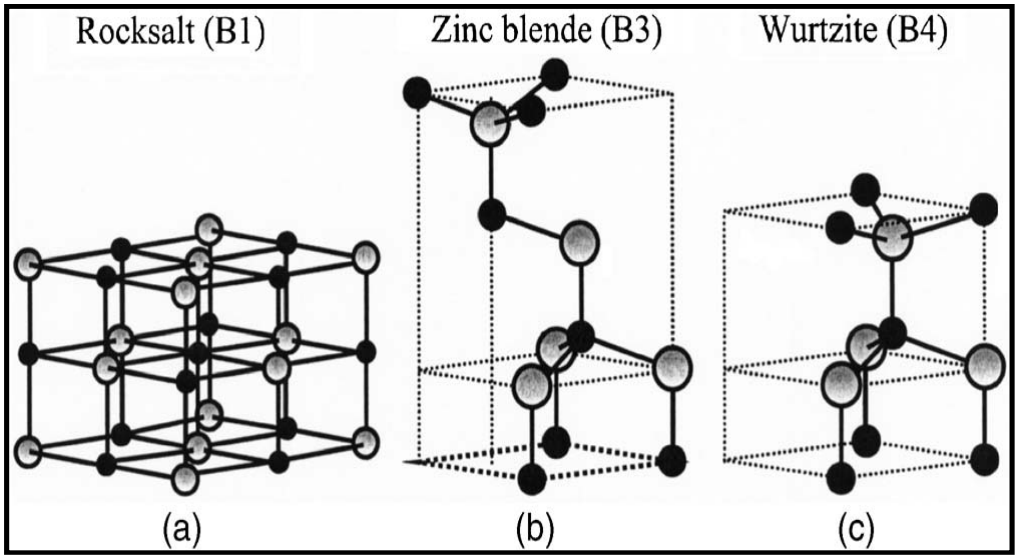

Figure 1.7: Ball and Stick Representation of ZnOCrystal Structures (a) Cubic Rock Salt (*B*1), (b) Cubic Zinc Blende (*B*3), and (c) Hexagonal Wurtzite(*B*4). The Shaded Grayand Black Spheres Denote Zn and O Atoms, Respectively.

Over the past decade, a significant amount of work has been done to improve the quality of ZnO single crystal substrates as well as grow its epitaxial films. The availability of large single crystals is one of the big advantages of ZnO over other compound semiconductors. The crystal structure of ZnO has wurtzite (B4), zinc blende (B3), and rock salt (B1), as schematically shown in Figure 1.7. At ambient conditions, the thermodynamically stable phase is wurtzite [16-24]. Irrespective of growth conditions ZnO is *n*-type due to oxygen vacancies or interstitials. In addition, ZnO has many other properties like high electron mobility, hexagonal wurtzite structure, high breakdown voltage, which are desirable for advanced semiconductor device applications. Another big advantage of ZnO is that it is very responsive to wet chemical etching, which facilitates the device design and fabrication [16-24]. Besides all of these, there are many more properties of ZnO like a large piezoelectric constant, a high thermal conductivity, and strong non-linear resistance of polycrystalline ZnO that has made ZnO in valuable for many of current technological applications. The values of the properties of ZnOare mentioned in the table 1.2.

Table 1.2: A Few Physical and Electrical Properties of ZnO[16-24]

Properties	Values
Crystal Structure	Wurtzite
Cleavage plane	<0001>
Lattice Constant	a=3.25 Å, c = 5.2 Å
Band Gap	3.37 eV (Direct Type)
Intrinsic Carrier Concentration	$3.11 \times 10^{-10} cm^{-3}$
Electron Mobility	$200\ cm^2\ V^{-1}\ s^{-1}$
Hole Mobility	$5\text{-}50\ cm^2\ V^{-1}\ s^{-1}$
Melting Point	1975 °C
Thermal Conductivity	$0.6\text{-}1\ W\ cm^{-1}\ °C^{-1}$
Bulk Modulus	$dyne\ cm^{-2}$
Refractive Index	2.008
Dielectric constant	8.5
Electron affinity	3.47 eV
Work function	5.07eV
Effective density of states in the conduction band, N_c	$2.2 \times 10^{18}\ cm^{-3}$
Effective density of states in the valence band, N_v	$1.8 \times 10^{19}\ cm^{-3}$
Effective mass of electron, m_e	$0.24\ m_0$
Effective mass of hole, m_h	$0.59\ m_0$

Similarly, apart fromZnO, two more oxide semiconductor materials have been chosen for this interface study, but in place of their semiconducting property their insulation property has been used. The lack of high-quality, thermodynamically-stable insulators with low interface states compelled the researchers to go for high-K materials for developing GaSb based devices. However, the major roadblock encountered was that

during the integration of the high-Kdielectric with the GaSb substrate,the surface of the GaSb gets oxidized to form traps at the high-K/GaSb interface [25]. Amongst the different high-K dielectrics, Al_2O_3showsasuperior interface with GaSb substrate, and hence ithasbeen studied intensively [26, 27]. Besides Al_2O_3 other high-K/GaSb interfaces like HfO_2/GaSb and HfAlO/GaSb with sulfur passivation have been studied very extensively [28]. In this thesis, the two high-K materials Al_2O_3& HfO_2 have beenused for the interface study. The properties of these high-K dielectrics,necessary to be known for the interface study are their permittivity, reverse breakdown voltage, bandgap etc.

Finally, for any kind of study to be performed on any device it is necessary to make proper contacts for providing the input signals and taking out the output electrical signals. The most commonly used metals for contact making purpose are silver (Ag), aluminium (Al), copper (Cu), platinum (Pt) etc. Here gold (Au) has been chosen in our experiment because it has certain advantages over theother materials.

1.3.3 Gold (Au)

In the interface study,gold (Au) has been chosen to make the contacts. Gold is preferred as it is one of the transition metals showing the least reactive nature under standard conditions. It occurs as a natural element, resistant to many acids, chemical reactions and corrosion. Gold provides excellent resistance against wear and tear, providing increased lifespan of the contact. Besides gold is not susceptible to fretting, because of which contact surfaces gradually wear out due to rubbing or any kind of friction. Furthermore, gold provides better protection against damage caused by heat. Though gold is a costly material, in addition toall the advantages mentioned before, it is easy to handle, smelt and fabricate [29].

1.4 Objective and scope of the work

This thesis focuses on the synthesis and characterisation of both bulk and thin film GaSb. These studies are imperative for the development ofa new classof electronics devices. In this section, studies of interfaces made by different materials are described.

To grow Gallium Antimonide bulk crystals,ThermoVertical Directional Solidification (TVDS) technique exclusively designed in our labhas beenused. This techniquedoes not need a crystal seed, the growth sample does notcome in contact with the

ampoule wall, the product does not need any coating material and external pressure is not needed. Besides these advantages this is a very simple, low cost technique and needs a well calibration of its temperature profile.

To deposit a GaSb thin film on a glass substrate, the Thermal Evaporation system was used.Sincethe melting point and vapour pressure of Ga and Sb are different, therefore, simultaneous evaporation of Ga and Sb materials using two evaporation systems do not produce a good stoichiometric compound. Therefore, to deposit a stoichiometric GaSb thin film on glass substratean alreadygrown GaSb sample was used as a single source material.

Once the bulk and thin film of GaSb material had beenprepared, the structural, morphological and electrical properties of the material were investigated to determinethe quality of the material, to test for its suitability in device fabrication. Apart from physical investigation, GaSb based devices were also validatedtheoretically. This was done to ensure the correctness of theexperimental characterisations. For theoretical analysis ATLAS TCAD software from SILVACO was used.

For metal-semiconductor interface analysis, a preliminary investigationwas carried out to obtain the electrical properties by characterisation of Au/n-GaSbSchottky diode (metal-semiconductor interface). It was also imperative to investigate the ideal behaviour of the Schottky contact using ATLASTCAD softwareprior to the fabrication. Therefore, both experimental and simulation studies were necessary to understand the metal-semiconductor interface for the proposed material for device application.

The device-worthiness of the deposited and characterized films neededto be evaluated again through the test vehicle of a heterostructure (semiconductor-semiconductor interface) device. Furthermore, structural and morphological analyses of the semiconductor films wererequiredto assess their material properties and quality. In addition,the electrical characterisation of the fabricated heterojunction was essential for understanding the conduction mechanism in *n*-ZnO/*p*-GaSbhetrostructure.

Since experimental fabricationof a Metal-Oxide-Semiconductor capacitor structure is beyond the capabilityof our infrastructural facilities,therefore, ATLAS TCAD tool was used for the study of the metal-oxide-semiconductor interface. In addition, the proposed techniques were used that are compatible withCMOS device fabrication.

1.5 Organization of Thesis

The main objective of this thesis was to growth, fabricate & characterisation of GaSb based devices. Therefore,the bulk GaSband thin filmGaSbsubstrates weregrownandcharacterised to ensure that it is device-worthy. Thereafter, these materials were used for electrical (especially interface) properties study and to ensure quality devices. For specific reasons discussed later, the Thermo Vertical Directional Solidification (TVDS) method was chosen for the bulk growth of GaSb. Thereafter, the Thermal Evaporation method was used to synthesise thin film GaSbout of the grown bulk GaSb. Subsequently, based on this material, both bulk crystal and thin films have been used for the fabrication of different devices and their electrical characterization. The experimental results have been then compared and validated by TCAD software. SILVACO-TCAD, the state-of-the-art simulation software available for academic purposes has been used for this study.From the point of view of developing devices, this thesishas beendivided into seven chapters including the introduction and conclusion for better presentation.

Chapter 1

The first chapter is the background of dissertation and prior art, which describes the different types of interfaces and their properties when different types of materials are placedin contact with each other. This chapter then focuses on the material set used in this thesis, particularly onGaSb and ZnO, and their properties are highlighted for their prospective use in devices in the field of electronics.

Chapter 2

In the second chapter, the synthesis of a bulk GaSbcrystal by the ThermoVertical Directional Solidification methodindigenously designed in our lab has beendescribed. The grown ingot was then taken out and a small piece of the sample was then taken for the depositionof a uniform GaSb thin film on a glass substrate by the Thermal Evaporation technique.

Chapter 3

Chapter 3 deals with the characterisation of the grown bulk GaSb and the GaSb film deposited byTVDS method and Thermal Evaporation technique respectively. This chapter describes the experimental characterisation of the material for the study of physical and electrical properties of the grown bulk and thin film GaSb. Experimental results have been

compared and validated by SILVACO ATLAS TCAD software, a state-of-art simulation software available for academic purpose.

Chapter 4

In this chapter, a preliminary investigation wasbeing made to obtain the interface properties of Au/n-GaSbSchottky diode. Current-Voltage (I-V) and Capacitance-Voltage (C-V) were chosen as a vehicle to find out interface properties like the barrier height and ideality factor. Besides an experimentally fabricated Schottky contact, a simulated Au/n-GaSbSchottky diode structure was also designed using ATLAS TCAD softwarefor validation. Furthermore,for the simulated Au/n-GaSb Schottky diode barrier height and ideality factor were found for a temperature range of 30K- 300K.

Chapter 5

This chapter contains a new method for deposition of ZnO film,on aGaSbfilm that is itself deposited on a glass substrate, by Chemically Wet and Dry (CWD) method indigenously designed in our lab to fabricate a heterojunction. Structural and morphological analysis of*n*-ZnO/*p*-GaSb heterojunction was studied to discuss the ZnO-GaSb interface in terms of lattice mismatch, probable existence of strain and critical thickness of ZnO film. For electrical analysis Magneto resistance measurement and Hall Effect measurement were done to study the band diagram and conduction mechanism of the heterojunction. From the literature survey this has been found that *n*-ZnO/*p*-GaSb heterojunction has been reported for the first time.

Chapter 6

In this chapter,the theoretical study of oxide-semiconductor interface in a MOSCAP, using ATLAS TCAD toolwas carried out, using the high frequency capacitance-voltage (C-V) characteristics. Theinterface properties were found using theTerman Method. High quality thermodynamically stable insulators like high-Ks (Al_2O_3, HfO_2) with low interface states were chosen.The surface of GaSb was passivated for the better integration of GaSb substrate with that of high-K oxides. Detailed interface studiesof MOSCAP structures, both with and without surface passivation were carried out.

Chapter 7

The last chapter summarises the work done in the thesis and highlights significant achievements and thereafter, thesis concludes with thescope of work for the future.