Chapter-3

Design and Development of PID and Auto Tuned PID Controllers

3.1 VI block diagram for PID control using Lab VIEW:

Design and development of VI diagram and front panel is one of the main features of the present work. The design and development of VI varies with application. This design is discussed in this section.

Functions, controls and tools palettes are opened in the file to select the required icons. A DBL terminal both on front panel and block diagram represents precision floating-point numeric control or indicator. A wire can be attached anywhere to it. Constants are terminals that supply fixed data to block diagram. User defined constants are constants that are defined before running VI DBL is used for keeping the set point of 1500 rpm as shown in the figure 3.1. The analog input channel (AI) is the DAQ sub VI that acquires a single value. In the present case, a raw voltage from Hall sensors is converted into frequency by using F / V converter which is expressed by the equation.

$$f_2 = a_1 V_0 + a_2$$

This equation is realized in the VI block diagram using adder and multiplier icons. In the present case, a_1 = 44.809, a_2 =0.759. This frequency is multiplied with '6' for converting it into speed. The output of this multiplier is the measured speed (process variable) of the BLDC motor. This is one of the inputs to the PID icon. Another input is set point. The PID parameters such as

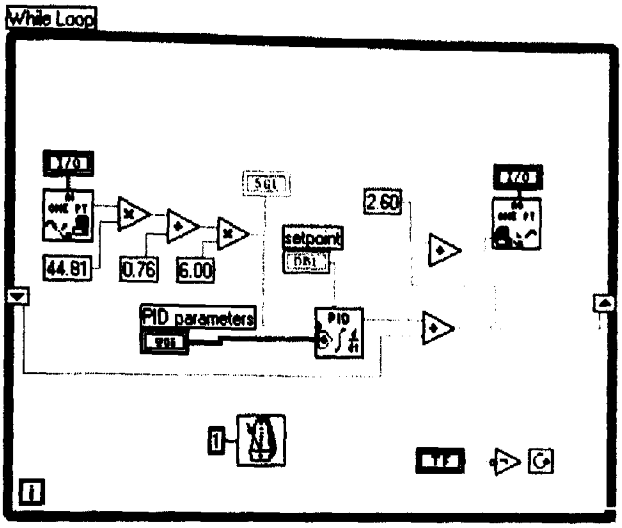

Figure3.1 : VI block diagram for the speed control of BLDC motor using convetional PID contoller

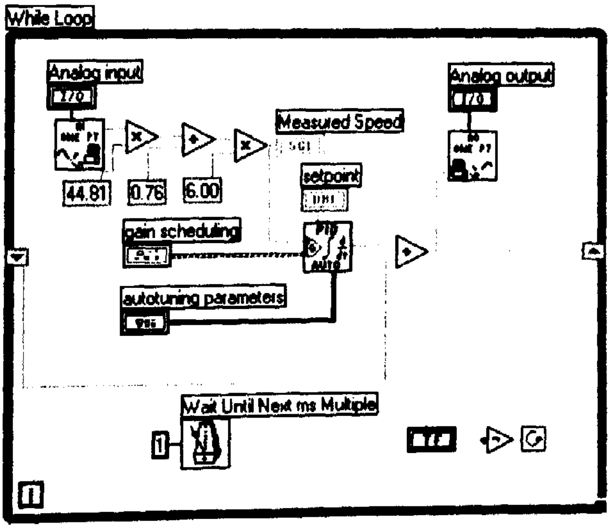

Figure 3.2: VI block diagram for the speed control of BLDC motor using Auto-tuned PID contoller

K_p (proportional gain), T_i (integral time) and T_d (derivative time) are fed to PID icon in the form of cluster. Depending upon the error and PID parameters, the PID controller gives out cu(k) (control output). This is added to process variable u(k−1) to get u(k)

i.e. u(k) = u(k−1) + cu(k).

This step is done using a shift register (represented by an arrow on both sides of while loop). An offset voltage of the IC UCC 3626 of 2.6 V is added to the u(k) using an adder icon. The resultant control voltage is fed to PWM controller IC UCC 3626 through DAQ board and SCXI 1124 card represented as I/O and Analog output (AO). All these computations are done in a while loop. The wait until next millisecond multiple labeled icon is used to control the loop timing, which determines the sampling time for the present application. Sampling time of 1msec has been used in the present work. The Boolean icon (represented as TF) and logic NOT are connected with the while loop, in order to control the iteration cycle of loop under process.

The PWM signals are fed to driver circuit, which in turn drives the BLDC motor and controls the speed by PID control.

3.2 Auto tuned PID CONTROLLER:

Auto tuning improves the performance of a controller. Often, due to poor tuning, many controllers may be too aggressive some may be too sluggish, when the process dynamic characteristics are not known, manual tuning is difficult. Hence auto tuning is needed.

The auto tuned PID controller VI uses Ziegler and Nichols heuristic method for determining the PID parameters (K_P, T_i and T_d). The PID parameters are determined from the knowledge of the critical gain, and the critical period. This VI is same as conventional PID controller VI, except the addition of auto tuning and PID gain scheduling parameters fig (3.2). The auto tuning parameters are the parameters used for the auto tuning purpose. Gain scheduling also is one of the parameters of the auto tuned PID controller icon. Gain scheduling describes a system where controller parameters changes depending upon the measured operating conditions. The gain scheduling parameter effectively and adaptively controls a system whose dynamics change with operating conditions.

3.3 Experimental Results and Discussion:

First, the PID parameters K_P, T_i and T_d are fixed to some values for a set point of 1500 rpm. Both set point and process variable are applied to PID. VI along with the initial PID parameters. PID parameters are tuned for achieving the pv = sp. The time taken for the motor to reach the set point 1500 rpm is observed to be 2.5 sec, without any over shoot/undershoots and zero steady state error.

These PID parameters are given to auto PID VI. Again time taken for the BLDC motor to reach the speed of 1500 rpm is observed. The parameters are varied to obtain the best response i.e. minimum settling time without overshoots/undershoots and zero steady state error.

The settling time for auto PID is 2.2 sec. The settling time for both PID and Auto PID methods for the speed control of BLDC motor is shown in the table 3.1. The experimental transient response of speed control of BLDC motor using PID and Auto Tuned PID controllers are as shown in fig 3.3

Table 3.1 Settling time for PID & Auto PID

S.No.	PID	Auto PID
1.	2.5 Sec	2.2 Sec

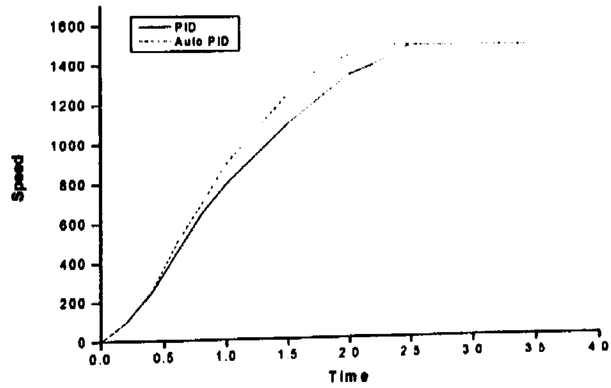

Fig 3.3 shows the experimental transient response of speed control of BLDC motor using PID and Auto Tuned PID controllers.

The experimental results reveal that Auto PID gives shorter settling time and better control, compared to the conventional PID.

In case of conventional PID controller the parameters K_P, T_i and T_d are manually varied for the set point speed. The experimental transient response was observed with a certain set of PID parameters. The transient response was observed to have large overshoots/undershoots with a large settling time with some steady state error. By tuning the PID parameters the overshoots/ undershoots were reduced, settling time is decreased. This tuning is continued till the steady state error becomes zero. The fine tuned PID parameters for a set point of 1500 rpm are as follows:

$K_P = 0.000081, T_i = 0.18 \;\; T_d = 0.08.$

The tuned PID parameters are given to auto tuned PID controller. The auto tuned PID controller automatically tunes the PID parameter for a set point. This results in adaptive controller for determining the PID parameters. The auto tuning of conventional PID parameters result in further reduction of settling time.