

TABLE OF CONTENTS

DECLARATION BY THE SCHOLAR

SUPERVISOR'S CERTIFICATE

ACKNOWLEDGEMENT

PREFACE

i

LIST OF ACRONYMS AND ABBREVIATIONS

iii

LIST OF FIGURES

v

LIST OF TABLES

viii

LIST OF PUBLICATIONS

x

CHAPTER-1 INTRODUCTION

1

1.1	COMPUTATION SCHEME FOR 1-D DWT.....	2
1.2	COMPUTATION SCHEME OF 2-D DWT.....	7
1.3	MULTILEVEL 2-D DWT.....	10
1.4	VLSI SYSTEM.....	13
1.5	THESIS ORGANIZATION.....	14

CHAPTER-2 LITERATURE REVIEW

2.1	PA AND RPA-BASED DESIGNS.....	15
2.2	FOLDED DESIGNS.....	16
2.3	PARALLEL DESIGNS	18
2.4	MULTIPLIER LESS DESIGNS.....	19
2.5	PROBLEM FORMULATION.....	25

**CHAPTER-3 PARALLEL ARCHITECTURE FOR MULTI-LEVEL LIFTING 2-D
DWT WITHOUT USING DATA-SELECTOR**

3.1	INTRODUCTION.....	27
3.2	DATA-ACCESS SCHEME.....	28
	3.2.1 STUDY ON DATA-FLOW OF MULTI-LEVEL LIFTING 2-D DWT...	29
	3.2.2 PROPOSED DATA-ACCESS SCHEME.....	33
3.3	BLOCK FORMULATION OF LIFTING 2-D DWT.....	35
3.4	PROPOSED ARCHITECTURE	39
	3.4.1 A GENERIC DESIGN OF J -TH PU.....	40
3.5	HARDWARE AND TIME COMPLEXITIES	45
	3.5.1 SYNTHESIS RESULTS.....	48
3.6	CONCLUSION.....	49

CHAPTER-4 EFFICIENT RADIX-8 BOOTH MULTIPLIER DESIGN

4.1	INTRODUCTION.....	50
4.2	REVIEW OF RADIX-4 BOOTH ALGORITHM.....	52
	4.2.1 MODIFIED RADIX-4 BOOTH MULTIPLICATION ALGORITHM.....	54
4.3	RADIX-8 BOOTH MULTIPLICATION ALGORITHM.....	58
	4.3.1 MODIFIED RADIX-8 BOOTH MULTIPLICATION ALGORITHM	60
	4.3.2 COMPLEXITY ANALYSIS	62
4.4	PROPOSED RADIX-8 BOOTH MULTIPLIER DESIGN.....	64
	4.4.1 MODIFIED 4:1 MULTIPLEXER DESIGN	64
	4.4.2 REGULAR PARTIAL PRODUCT ARRAY.....	66
	4.4.3 PROPOSED DESIGN	69

4.5	HARDWARE AND TIME COMPLEXITIES.....	73
	4.5.1 HARDWARE COMPLEXITY	73
	4.5.2 CRITICAL PATH DELAY (CPD).....	74
	4.5.3 PERFORMANCE COMPARISON	75
4.6	SYNTHESIS RESULTS.....	76
4.7	CONCLUSION	77

**CHAPTER-5 CONSTANT RADIX-8 BOOTH MULTIPLIER AND EFFICIENT
LIFTING 2-D DWT ARCHITECTURE**

5.1	INTRODUCTION.....	78
5.2	PROPOSED RADIX-8 FIXED-WIDTH BOOTH MULTIPLIER DESIGN	81
	5.2.1 GENERIC CONSTANT BOOTH MULTIPLIER.....	81
	5.2.2 FIXED-WIDTH RADIX-8 BOOTH MULTIPLIER DESIGN.....	82
	5.2.3 HARDWARE-TIME COMPLEXITIES OF RADIX-4 AND RADIX-8 ...	83
	5.2.4 COMPARISON OF SYNTHESIS RESULT.....	85
5.3	PROPOSED LIFTING STRUCTURE OF 2-D DWT	87
5.4	HARDWARE COMPLEXITY OF LIFTING 2-D DWT STRUCTURE.....	94
5.5	CONCLUSION	97

**CHAPTER-6 LUT-MULTIPLIER-BASED BLOCK LIFTING 2-D DWT
STRUCTURE**

6.1	INTRODUCTION.....	98
6.2	PROPOSED LUT MULTIPLIER DESIGN.....	99
6.3	PROPOSED LUT MULTIPLIER BASED LIFTING DWT STRUCTURE.....	107
6.4	AREA-DELAY COMPLEXITIES.....	110

6.5	CONCLUSION.....	111
-----	-----------------	-----

CHAPTER-7 CONCLUSION & FUTURE SCOPE

7.1	CONCLUSION.....	112
-----	-----------------	-----

7.2	FUTURE SCOPE.....	116
-----	-------------------	-----

	BIBLIOGRAPHY	118
--	---------------------	------------

