

REFERENCES

1. Meixia Duan, Hongling Han, Research and Implementation of Gigabit Ethernet Full Line Rate, Cross Strait Quad-Regional Radio Science and Wireless Technology Conference, 2011, pp. 736-738.
2. Gigabit Ethernet Technology and Solutions, Copyright © 2001, Intel Corporation.
3. Gerd Keiser, Local Area Network, Tata McGraw-Hill , Second Edition, 2002.
4. <http://support.microsoft.com/kb/103884>
5. Behrouz A. Forouzan, Data Communication and Networking, Tata McGraw-Hill , 4th Edition, 2008.
6. <http://www.ieee802.org/dots.shtml>
7. Fundamentals of Ethernet: 10 Megabit Ethernet to 10 Gigabit Ethernet , JDSU, (www.jdsu.com/test).
8. Robert Metcalfe, David Boggs, Ethernet: Distributed packet switching for local computer networks, Association for Computing Machinery, Vol.19, No.5, July 1976.
9. <http://timeline.ethernethistory.com>.
10. Phil Edholm, Paul Littlewood, Next-generation Ethernet:The key to infrastructure transition, Nortel Technical Journal, Issue 4, pp. 7-24.
11. <http://archiv.cesnet.cz/doc/techzpravy/2010/100ge-study/#phys-layer>
12. Carrier sense multiple access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, IEEE Std 802.3™ 2008.
13. William Stallings, Gigabit Ethernet, The Internet Protocol Journal – Vol. 2, No. 3,September 1999, pp. 21-25.
14. AnySpeed Ethernet MAC Core Product Brief Version 1.0, August 2005, 1, MorethanIP GmbH, Muenchner Str. 199, 85757 Karlsfeld, Germany.
15. Alan F. Benner, Petar K. Pepeljugoski, Renato J. Recio, A Roadmap To 100g Ethernet At The Enterprise Data Center, IBM Corp, IEEE Applications & Practice, November 2007, pp. 10-17.
16. Neil Mcallister, Networking Industry To Collaborate On Terabit Ethernet, 20 Aug 2012, (http://www.theregister.co.uk/data_centre/hpc/).
17. Wayne Rash, Terabit Ethernet Is in Your Future, March 26, 2010, (<http://www.eweek.com/networking/terabit-ethernet-is-in-your-future/#sthash.IM6Sr5Y4.dpuf>).
18. Oleh et al., Terabit Ethernet: Ambitious or Reality For High Speed Network At Future, 2010, (<http://www.ptmk.ump.edu.my> › Artikel ICT › Rangkaian).
19. Finkler, S. Sidhu, D., Performance analysis of IEEE 802.3z Gigabit Ethernet Standard, Global Telecommunications Conference, 1999, GLOBECOM '99 , Vol. 2, pp. 1302-1306.
20. Tinoosh Mohsenin , Thesis: Design and Evaluation of FPGA-Based Gigabit-Ethernet/PCI Network Interface Card, Rice University, 2004.
21. A. Chaubal, Thesis: Design and Implementation of an FPGA-based Partially Reconfigurable Network Controller, Bradley Department of Electrical and Computer Engineering Blacksburg, Virginia, 2004.
22. M. Ciobotaru, et al., Versatile FPGA-based Hardware Platform for Gigabit Ethernet Applications, 6th Annual Postgraduate Symposium, Liverpool, UK, June 2005.

23. A. Bianco et al., Boosting the performance of PC-based softwares routers with FPGA-enhanced line cards, Politecnico di Torino, 10129 Torino.
24. J. Shafer, S. Rixner, RiceNIC: A reconfigurable net-work interface for experimental research and education, Proc. of the Workshop on Experimental Computer Science (ExpCS'07), June 2007.
25. Zou et al., Co-Design For An SoC Embedded Network Controller, Journal of Zhejiang University, Science A, ISSN 1009-3095 (Print), 2006, pp. 591-596.
26. Dilip Thomas, K.S. Mohanachandra Panicker, VLSI Implementation Of Gigabit Ethernet With Data Compression And Decompression, IET-UK International Conference on Information and Communication Technology in Electrical Sciences (ICTES 2007), M.G.R. University, Chennai, Tamil Nadu, India, December 2007, pp.826-826.
27. Dave Bailey, Richard Hughes-Jones, Marc Kelly, Using FPGAs to Generate Gigabit Ethernet Data Transfers and Studies of the Network Performance of DAQ Protocols, The University of Manchester, UK. , (<http://www.docstoc.com/docs/38636314/Using-FPGAs-to-Generate-Gigabit>).
28. G. A. Covington, G. Gibb, J. Lockwood, N. McKeown, A packet generator on the netfpga platform, Proc. In The 17th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, April 2009.
29. Nicholas Tsakiris, Greg Knowles, Gigabit IP Core for Embedded Systems, International Journal Of Circuits, Systems And Signal Processing, Vol.2, No.2, 2008 p. 347.
30. T. V. Ramabadran, S. S. Gaitonde, A Tutorial on CRC Computations, IEEE Micro, Vol.8, No. 4, August 1988, pp. 62-75.
31. G. Albertango, R. Sisto, Parallel CRC Generation, IEEE Micro, Vol. 10, No. 5, October 1990, pp. 63-71.
32. T. B. Pei, C. Zukowski, High-speed parallel CRC circuits in VLSI, IEEE Transactions on Communications, Vol. 40, No. 4, Apr. 1992, pp. 653 - 657.
33. G. Castagnoli, S. Brauer, M. Herrmann, Optimization of cyclic redundancy-check codes with 24 and 32 parity bits, IEEE Transactions on Communications, Vol. 41, No.6, June 1993, pp. 883 -892.
34. Sait S.M., Tanvir, M.S.K., VLSI Layout Generation Of A Programmable CRC Chip, IEEE Transactions on Consumer Electronics, Vol.39, No.4, November 1993, pp. 911 – 916.
35. U. Nordqvist, T. Henriksson, D. Liu, CRC Generation for Protocol Processing, Norchip, 2000, Turku, Finland, pp. 288-293.
36. A. Perez, Byte-wise CRC Calculations, IEEE Micro, Vol. 3, No. 3, June 1983, pp. 40-50.
37. Ming-Der Shieh, Ming-HwaSheu, Chung-Ho Chen, Hsin-Fu Lo, A Systematic Approach for Parallel CRC Computations, Journal Of Information Science And Engineering, Vol. 17, 2001, pp. 445-461.
38. R. Nair, G. Ryan, F. Farzaneh, A Symbol Based Algorithm for Implementation of Cyclic Redundancy Check (CRC), In Proc. of VHDL International Users' Forum, 1997, pp. 82 -87.
39. Tridib Chakravarty, Performance of Cyclic Redundancy Codes for Embedded Networks, MS Report, Dept. of Elect. & Comp. Engg., Carnegie Mellon University, December 2001.
40. Koopman, P., 32-bit cyclic redundancy codes for Internet applications, Intl. Conf. Dependable Systems and Networks (DSN), Washington DC, July 2002, pp.459-468.
41. Giuseppe Campobello, Giuseppe Patane, Marco Russo, Parallel CRC Realization, IEEE Transactions On Computers, Vol. 52, No. 10, October 2003.
42. Philip Koopman, TridibChakravarty, Cyclic Redundancy Code (CRC) Polynomial Selection For Embedded Networks, The International Conference on Dependable Systems and Networks, DSN-2004, (http://users.ece.cmu.edu/~koopman/roses/dsn04/koopman04_crc_poly_embedded.pdf).

43. Baicheva, T., S. Dodunekov, P. Kazakov, On The Cyclic Redundancy-Check Codes With 8-Bit Redundancy, *Computer Communications*, Vol. 21, 1998, pp. 1030-1033.
44. Chao Cheng, K.K. Parhi, High-Speed Parallel CRC Implementation Based On Unfolding, Pipelining and Retiming, *IEEE Transactions On Circuits And Systems*, Vol. 53, No. 10, Oct. 2006, pp. 1017 – 1021.
45. M. Walma, Pipelined Cyclic Redundancy Check (CRC) calculation, *ICCCN 2007*, In Proc. of 16th International Conference on Computer Communications and Networks, Honolulu, HI, USA, 2007, pp. 365 - 370.
46. Kazakov, P., Fast calculation of the number of minimum-weight words of CRC codes, *IEEE Trans. Information Theory*, Vol.47, No.3, March 2001, pp. 1190-1195.
47. H. Michael Ji., Earl Killian, Fast Parallel CRC Algorithm and Implementation on a Configurable Processor, *ICC 2002*, IEEE International Conference on Communications, Vol.3, 2002, pp. 1813 – 1817.
48. Tomas Henriksson, Dake Liu , Implementation of Fast CRC Calculation, *Proceedings of the ASP-DAC 2003, Asia and South Pacific*, Jan. 2003, pp. 563 – 564.
49. Tomas Henriksson, In-Line CRC Calculation and Scheduling for 10 Gigabit Ethernet Transmission, (http://www.da.isy.liu.se/pubs/tomhe/SSoCC2002_crc.pdf).
50. Ulf Nordqvist, Tomas Henrikson, Dake Liu, Configurable CRC Generator, Department of Electrical Engineering, Linköpings University Linköpings, Sweden, (<http://www.da.isy.liu.se/pubs/ulfnor/ulfnor-ddecs2002.pdf>).
51. M. Braun, J. Freidich, T. Grun, J. Lembert, Parallel CRC computation in FPGAs, In Proc. of Workshop on Field Programmable Logic Application, 1996, pp. 156-165.
52. Yan Sun and Min Sue Kim, A table based algorithm for pipelined CRC calculation, In Proc. of Communications (ICC), 2010 IEEE International Conference, Cape Town, South Africa, 2010, pp. 1 - 5.
53. D. J. C. MacKay, R. M. Neal, Near Shannon limit performance of low density parity check codes, *Electronics Letters*, vol. 32, pp. 1645–1646, Aug. 1996. Reprinted *Electronics Letters*, Vol 33, No. 6, 13th March 1997, pp. 457–458
54. M. Davey , David J.C. Mackay, Low Density Parity Check Codes over GF(q), Cavendish Laboratory, Cambridge, UK, June 1998, (<http://citeseerx.ist.psu.edu/viewdoc>).
55. C. J. Howland, A. J. Blanksby, Parallel decoding architectures for low density parity check codes, In Proc. IEEE ISCAS, Vol. 4, May 2001, pp. 742–745.
56. R. Gallager, Low-density parity-check codes, *IEEE Trans. Inf. Theory*, Vol. IT-8, No. 1, Jan. 1962, pp. 21–28.
57. D. MacKay, R. Neal, Good codes based on very sparse matrices., *IMA Conf. Cryptography and Coding*, 1995, (<http://www.cs.toronto.edu/~mackay/mnc4s.pdf>).
58. D. MacKay, Good error correcting codes based on very sparse matrices, *IEEE Trans. Information Theory*, Vol. 47, No. 5, 2001, pp. 399-431.
59. B. Levine, R. Reed Taylor , Herman Schmit, Implementation of Near Shannon Limit Error-Correcting Codes Using Reconfigurable Hardware , In Proc. of IEEE Symposium on Field-Prog. Cust. Comput. Mach 2000, pp. 217-226.
60. T. J. Richardson, R. L. Urbanke, The capacity of low-density parity-check codes under message-passing decoding, *IEEE Trans. Inf. Theory*, Vol. 47, No. 2, Feb. 2001, pp. 599–618.
61. Tong Zhang, Keshab Parhi, Joint Code and decoder design for implementation-oriented (3,k) – regular LDPC codes, Published in *Signals, Systems and Computers*, 2001. Conference Record of the Thirty-Fifth Asilomar Conference on, Vol. 2, Nov. 2001, pp.1232-1236.

62. Yeo et al., High Throughput Low-Density Parity-Check Decoder Architectures, In Proc. of the IEEE GLOBECOM 2001, IEEE Press, pp. 3019 -3024.
63. Hisashi Futaki, Tomoaki Ohtsuki, Performance of Low-Density Parity-Check (LDPC) Coded OFDM Systems, Published in Vehicular Technology Conference, 2001. VTC 2001 Fall. IEEE VTS 54th, Vol.1, 2001, pp. 82-86.
64. Hisashi Futaki, Tomoaki Ohtsuki, Low-Density Parity-Check (LDPC) Coded OFDM Systems with M-PSK, Published in Vehicular Technology Conference, 2002, VTC Spring 2002, IEEE 55th, Vol.2, 2002, pp. 1035-1039.
65. Blanksby , Howland, A 690-mW 1-Gb/s 1024-b, Rate-1/2 Low-Density Parity-Check Code Decoder , IEEE J. Solid State Circuits, Vol. 37, No. 3, 2002, pp. 404–412.
66. Ki-Moon Lee , Hayder Radha, The Design of the Maximum-Likelihood Decoding Algorithm of LDPC Codes over BEC Dept. of Math, Michigan State University, (citeseerx.ist.psu.edu/viewdoc).
67. David Burshtein, Gadi Miller, An Efficient Maximum-Likelihood Decoding of LDPC Codes Over the Binary Erasure Channel, IEEE Trans. Inform. Theory, Vol.50, 2004, pp. 2837-2844.
68. H. Xiao, A. H. Banihashemi, Improved Progressive-Edge-Growth (PEG) Construction of Irregular LDPC Codes, IEEE Comm. Letters, Vol. 8, No. 12, December 2004, pp. 715-717.
69. Yang Sun, Marjan Karkooti, Joseph R. Cavallaro, High Throughput, Parallel, Scalable Ldpc Encoder/Decoder Architecture For Ofdm Systems, Published in Design, Applications, Integration and Software, IEEE Dallas/CAS Workshop on, October 2006, pp. 39-42.
70. K. Shuaib et al., Performance evaluation of IEEE 802.15.4: Experimental and Simulation Results, Journal of Communications, Vol. 2, No. 4, June 2007, pp. 29–37.
71. C. P. Fewer, M. F. Flanagan, A. D. Fagan, A versatile variable rate LDPC codec architecture, IEEE Transaction on Circuits Systems-I, Vol. 54, No.10, October 2007, pp. 2240–2251.
72. V.S. Ganepola, R.A. Carrasco , I. J. Wassell, Le Goff, Performance study of Non-binary LDPC Codes over GF(q), Sch. of Electr., Univ. of Newcastle, Newcastle, (<http://www.cl.cam.ac.uk/research/dtg/publications/public/ic231/40862.pdf>).
73. Hua Xiao, Amir H. Banihashemi, Estimation of Bit and Frame Error Rates of Finite-Length Low-Density Parity-Check Codes on Binary Symmetric Channels, IEEE Trans. in Communications, Vol. 55 , No. 12, Dec. 2007, pp. 2234 – 2239.
74. Hua et al., Estimation of Bit and Frame Error Rates of Finite-Length Low-Density Parity-Check Codes on Binary Symmetric Channels, June 2009, (citeseerx.ist.psu.edu/viewdoc).
75. Zhou Zhong et al., Wang Modified Min-sum Decoding Algorithm for LDPC Codes Based on Classified Correction, Published in Proceedings of ChinaCom Conference, Aug. 2008, pp. 932 – 936.
76. Syed Aziz, Mahfuzul, Minh Duc Pham, Duc, Implementation Of Low Density Parity Check Decoders Using A New High Level Design Methodology, Journal Of Computers, Vol. 5, No. 1, January 2010, pp. 81-90.
77. Md. Murad Hossain et al., Modified Log Domain Decoding Algorithm for LDPC Codes over GF (q), Journal of Selected Areas in Telecommunications (JSAT), June 2011, pp. 30-36.
78. Yeo et al., Architectures and Implementations of Low-Density Parity Check Decoding Algorithms , IEEE International Midwest Symposium on Circuits and Systems, Vol.3, August 2002, pp. 437-440.
79. Zhang et al., Design of LDPC Decoders for Low Error Rate Performance , Published in IEEE Transactions on Communications, Vol.57 , No. 11, Nov. 2009, pp. 3258 – 3268.
80. Yang et al., 428-Gb/s single-channel coherent optical OFDM transmission over 960-km SSMF with constellation expansion and LDPC coding, Optics Express, Vol. 18, No. 16, August 2010, pp. 16883-16889.

81. Zhang et al., Evaluation of four-dimensional nonbinary LDPC-coded modulation for next-generation long-haul optical transport networks, *Optics Express*, Vol. 20, No. 8, April 2012, pp. 9296-9301.
82. Tao Jin-jing et al., Application of LDPC codes in atmospheric optical communication with coherent detection, *Optoelectronics letters*, Vol. 9, No. 2, March 2013, pp. 132-134.
83. Arun Kumar, Rajendar Bahl, An Architecture for High data rate Very Low Frequency communication, *Defence Science Journal*, 2013, Vol. 63, No.1, pp.25-33.
84. Jianguo Yuan et al., A new construction method of LDPC codes for optical transmission systems, *Frontiers of optoelectronics*, Vol. 5, No.3, Sept. 2012, pp. 311-316.
85. Yuan Jianguo et al., A novel construction algorithm of the LDPC code for high-speed long-haul optical transmission systems, *Optic International J. for Light & Electron Optics*, Vol.124, No.18, September 2013, pp. 3181-3186.
86. L. B. James, A. W. Moore, M. Glick, Structured Errors in Optical Gigabit Ethernet, Passive and Active Measurement Workshop (PAM 2004), Antibes Juan-les-Pins, France, Published in book *Passive and Active Network Measurement* by Springer-Verlag Berlin Heidelberg, pp. 195-204.
87. L. B. James et al., Packet error rate and bit error rate non-deterministic relationship in optical network applications, Univ of Cambridge, UK, 2005, (www.cl.cam.ac.uk/~awm22/publications/james2005packet.pdf).
88. A. Xiang et al., Design and verification of an FPGA-based bit error rate tester , *Proceedings in TIPP 2011*, Published by Elsevier, 2012, pp. 1875-3892 doi: 10.1016/j.phpro.2012.02.492.
89. Frazier, Johnson, Gigabit Ethernet: From 100 to 1,000 Mbps, *IEEE Internet Computing*, Jan. 1999, (<http://www.gigabit-ethernet.org>).
90. Introduction to Gigabit Ethernet, Technology brief, Copyright © 2000 Cisco Systems, Inc.
91. http://opencores.org/project,ethernet_tri_mode.
92. M. Ciobotaru, et al., Versatile FPGA-based Hardware Platform for Gigabit Ethernet Applications, 6th Annual Postgraduate Symposium, Liverpool, UK, June 2005, (cern.ch/ciobota/papers/2005_getb_liverpool.pdf).
93. Zou et al., Co-design for an SoC embedded network controller, *Journal of Zhejiang University SCIENCE A*, 2006, pp. 591-596.
94. C. Kachris, et al., Design and performance evaluation of an adaptive FPGA for network applications, *Microelectron. J* , 2008, doi:10.1016/j.mejo.2008.05.01.
95. Stratix II GX Device Handbook, Volume 2 © 2007 Altera Corporation SIIGX5V2-4.3.
96. Triple Speed Ethernet Data Path Reference Design AN-483-June 2009 ver. 1.1 Altera Corporation.
97. Triple-Speed Ethernet MegaCore Function User Guide © December 2010 Altera Corporation
98. Stallings, William, *Data and computer communications*, Upper Saddle River, N.J. : Pearson/Prentice Hall, 8th Edition, 2007.
99. Palani Subbaiah, Bit- Error Rate for High Speed Serial Data Communication, Data-communications Division, Cypress Semiconductor, November 2008, (www.pdfgeni.me/pdf/b6a80fe2e0)
100. ATM Shafiu Alam, Effect of Additive White Gaussian Noise (AWGN) on the Transmitted Data, Department of Electrical, Computer and Communications Engineering, London South Bank University , Dec 2008, (atmshafiualam.webs.com/IDC-Ex-3-additive_white_Gaussian_noise.pdf).
101. http://en.wikipedia.org/wiki/Binary_symmetric_channel

- 102.[http:// www.dsplog.com/2007/08/05/bit-error-probability-for-bpsk-modulation/](http://www.dsplog.com/2007/08/05/bit-error-probability-for-bpsk-modulation/)
- 103.Peterson, W. & E. Weldon, Error-Correcting Codes, Second Edition, MIT Press, 1972.
- 104.Ulf Nordqvist, Thesis: Protocol Processing in Network Terminals, Department of Electrical Engineering , Linkopings University, SE-581 83 Linkoping , Sweden 2004.
- 105.Koopman, 32-bit cyclic redundancy codes for Internet applications, Intl. Conf. Dependable Systems and Networks (DSN), 2002, pp.459-468.
- 106.V. R. Gad, R. S. Gad, G. M. Naik, Implementation of Gigabit Ethernet using Double CRC-32 technique, Symposium on VLSI & Embedded System, Goa University & VSI , Goa Chapter, Feb 2010.
- 107.U. Nordqvist, T. Henriksson, D. Liu, CRC Generation for Protocol Processing, Norchip 2000, Turku, Finland, pp. 288-293.
- 108.Ming-Der Shieh, Ming-Hwa Sheu, Chung-Ho Chen, Hsin-Fu Lo , A Systematic Approach for Parallel CRC Computations, Journal Of Information Science And Engineering, Vol. 17, 2001 pp. 445-461.
- 109.Giuseppe Campobello, Giuseppe Patane,Marco Russo , Parallel CRC Realization, IEEE Transactions On Computers, Vol. 52, No. 10, 2003, pp. 245-256.
- 110.Luben, Cavannay, The iSCSI CRC32C Digest and the Simultaneous Multiply and Divide Algorithm, USA ,Jan. 2002, (www.research.ibm.com/haifa/satran/ips/Vince-Luben-crc32c-01.pdf) .
- 111.Luben, Cavannay, The iSCSI CRC32C Digest and the Simultaneous Multiply and Divide Algorithm, USA , Jan. 2002, (www.research.ibm.com/haifa/satran/ips/Vince-Luben-crc32c-01.pdf).
- 112.Kounavis, M.E., Berry, F.L., Novel Table Lookup-Based Algorithms for High-Performance CRC Generation, IEEE Transactions on Computers, Vol. 57, No. 11, 2008, pp. 1550-1560.
- 113.Gam D. Nguyen , Fast CRCs, IEEE Transactions On Computers, Vol. 58, No. 10, Oct. 2009, pp. 1321-1331.
- 114.Ulf Nordqvist, Thesis: Protocol Processing in Network Terminals, Department of Electrical Engineering , Linkopings University, SE-581 83 Linkoping , Sweden 2004.
- 115.Ji. H. Michael, Killian E., Fast parallel CRC algorithm and implementation on a configurable processor, IEEE Int. Conf. on Communications, ICC 2002, Vol. 3, 2002, pp. 1813-1817.
- 116.Weidong Lu, Stephan Wong, A Fast CRC Update Implementation, The Netherlands International Journal of Innovative Technology and Exploring Engineering (IJITEE), Vol. 3, No.1, October 2013, pp. 113-120.
- 117.Grymel, Furber, A Novel Programmable Parallel CRC Circuit, IEEE Transactions on VLSI Systems , Vol. 19, No.10, 2011, pp. 1898-1902.
- 118.Toal et al., Design and Implementation of a Field Programmable CRC Circuit Architecture, IEEE Transactions on VLSI Systems, Vol.17, No. 8, 2009, pp. 1142-1147.
119. James E. Gilley, Bit-Error-Rate Simulation Using Matlab, Transcrypt International, Inc., 2003, (wr.lib.tsinghua.edu.cn/sites/default/files/1195180204498.pdf) .
- 120.Ivan B. Djordjevic, Bane Vasic, LDPC-coded OFDM in fiber-optics communication systems, J. Of Optical Networking, Vol. 7, No. 3, March 2008, pp. 217-226.
- 121.Chin-Kuang Lian, A partially parallel LDPC decoder with reduced memory for long code length, Dept. of Elect. Engg., National Central University, , Taiwan, (www.researchgate.net) .
- 122.D. MacKay, R. Neal, Good codes based on very sparse matrices., IMA Conf. Cryptography and Coding, 1995, (<http://www.cs.toronto.edu/~mackay/mnc4s.pdf>).
- 123.D. MacKay, Good error correcting codes based on very sparse matrices, IEEE Trans. Information Theory, Vol. 47, No. 5, 2001, pp. 399-431.
- 124.N. Alon ,M. Luby, A linear time erasure-resilient code with nearly optimal recovery, IEEE Trans. Inf. Theory, Vol. 42, No. 6, Nov. 1996, pp. 1732–1736.

125. T. J. Richardson, R. L. Urbanke, The capacity of low-density parity-check codes under message-passing decoding, *IEEE Trans. Inf. Theory*, Vol. 47, No. 2, Feb. 2001, pp. 599–618.
126. T. J. Richardson, M. A. Shokrollahi, R. L. Urbanke, Design of capacity-approaching irregular low-density parity-check codes, *IEEE Trans. Inf. Theory*, Vol. 47, No. 2, Feb. 2001, pp. 619–637.
127. S. Chung, G. Forney, T. Richardson, R. Urbanke, On the design of low-density parity-check codes within 0.0045 db of the Shannon limit, *IEEE Commun. Lett.*, Vol. 5, No. 2, Feb. 2001, pp. 58–60.
128. Lin, Costello, *Error Control Coding: Fundamentals and Applications*, New Jersey: Prentice Hall, 2nd Edition, 2004.
129. B. Reiffen, Sequential Decoding for Discrete Input Memoryless Channels, *IRE Trans. Inf. Theory*, Vol. 8, No. 3, April 1962, pp. 208–220.
130. A. J. Blanksby, C. J. Howland, A 690-mW 1-Gb/s 1024-b, rate-1/2 low-density parity check code decoder, *IEEE J. Solid State Circuits*, Vol. 37, No. 3, 2002, pp. 404–412.
131. Bernhard M. J. Leiner, LDPC codes - a Brief Tutorial, April 2005 (www.bernh.net/media/download/papers/ldpc.pdf).
132. Eckford, Kschischang, Pasupathy, Analysis of Low-density Parity-check Codes for the Gilbert-Elliott Channel, *IEEE Trans. Inf. Theory*, Vol. 51, No. 11, Nov. 2005, pp. 3872–3889.
133. Vijay Nagarajan, Stefan Laendner, Olgica Milenkovic, High-throughput VLSI Implementations of Iterative Decoders and Related Code Construction Problems, *Journal of VLSI Signal Processing*, Vol. 49, 2007, pp. 185–206.
134. Marjan Karkooti, Thesis: Semi-Parallel Architectures for Real-time LDPC encoding, Houston, Texas, 2004.
135. L. Ping, W.K. Leung, Decoding low density parity check codes with finite quantization bits, *IEEE Comm. Letters*, Vol. 4, No.2, Feb. 2000, pp. 62–64.
136. H. Wymeersch, H. Steendam and M. Moeneclaey, Computational complexity and quantization effects of decoding algorithms of LDPC codes over GF(q), In Proc. ICASSP, Montreal, Canada, May 2004, pp. 772–776.
137. X. Hu, E. Eleftheriou, D.-M. Arnold, A. Dholakia, Efficient implementations of the sum-product algorithm for decoding LDPC codes, In Proc. IEEE Globecom, San Antonio, TX, Vol. 2, November 2001, pp. 1036–1036E.
138. M. Davey, David J.C. Mackay, Low Density Parity Check Codes over GF(q), Cavendish Laboratory, Cambridge, UK, June 1998, (<http://citeseerx.ist.psu.edu/viewdoc>).
139. J. Berkmann, On turbo decoding of nonbinary codes, *IEEE Comm. Letters*, Vol. 2, No. 4, April 1998, pp. 94–96.
140. H. Wymeersch, H. Steendam, M. Moeneclaey, Log-domain decoding of LDPC codes over GF(q), In Proc. IEEE Intern. Conf. on Commun., Vol. 2, No.2, June 2004, pp. 772–776.
141. Dan Dechene, Kevin Peets, Thesis: Simulated Performance of Low-Density Parity-Check Codes: A Matlab implementation, Lakehead University, Faculty of Engineering, 2006.
142. www.mathworks.in/matlabcentral/.../8977-ldpc-code-simulation.
143. W. E. Ryan, An Introduction to LDPC Codes, in *CRC Handbook for Coding and Signal Processing for Recording Systems* (B. Vasic, ed.), CRC Press, 2004.
144. 10 Gigabit Ethernet Technology Overview and Applications for Enterprise Data Centers, Blade network technologies, ©2009 BLADE Network Technologies, Inc., 2009.