CHAPTER 1

INTRODUCTION TO ETHERNET TECHNOLOGIES

1.1 Introduction

There has been a rapid development in the global information infrastructure and also a growing increase in the bandwidth requirements. Gigabit Ethernet is used not only for interconnection of computers, but also in high-speed network equipment as well as user access to metropolitan area network. It is also a popular and robust networking protocol for computer networks, backbone and industrial applications [1]. Ethernet has been successful for over 30 years because the Ethernet standards have progressed along with networking and bandwidth requirements. This progression of standards provides an obvious and straightforward migration path for companies as their bandwidth requirements increase[2]. Gigabit Ethernet has evolved from the original 10Mbps Ethernet standard, 10BASE-T, and the 100Mbps Fast Ethernet standards, 100BASE-TX and 100BASE-FX. The IEEE adopted Gigabit Ethernet over fiber optic cabling, IEEE 802.3z in June 1998 and its implementation was extensively supported by networking vendors. This standard helped the companies to improve traffic flow in congested areas. The IEEE standardized IEEE 802.3ab Gigabit Ethernet over copper as 1000BASE-T in June 1999, which enabled Gigabit speeds to be transmitted over Cat-5 cable.

Ethernet can be used with fiber optic cable in 550M and 5Km lengths and Cat-5 copper cable up to 100 meters. Gigabit connections can also be established for lengths of up to 70Km through use of long-haul Gigabit Interface Connectors (LH GBICs) in switches. Fiber is normally used between buildings or vertical connections between floors, where distances more than 100- meters are required. Copper cable is susceptible to electromagnetic interference, which can corrupt data whereas fiber provides immunity from environmental noise and security from unauthorized access to information. Multiple applications are simultaneously used on the desktops in today's enterprise. Certain applications such as online backup and recoveries of data and applications, large file transfers from data center servers and storage plants have an effect on the traffic related with all other applications that are using network resources at the same time.Thus deployment of Gigabit Ethernet to the desktop has improved the productivity

and performance of the enterprise. Similarly, data and information used in the decision-making process is extracted, delivered, and analyzed at significantly faster rates. However, as these applications become more advanced, they also become more bandwidth-intensive.

As more traffic is generated, network performance decreases, and so does employee productivity. Today, users may have one application in the foreground and several applications active in the background. Each user has his own computing requirement which is a combination of different applications requiring computer processor power and network bandwidth. The aggregate of the application traffic patterns should be applied to the available bandwidth,which reflects the true bandwidth and network use of the users and their applications. Large file transfers, multicast or on-demand video, e-mail with large attachments, on-demand backups and recovery, enterprise resource planning, customer relationship management and Web and Java-based tools, are among the list of applications that users run every day, without realizing much about it. Each user has unique traffic patterns and bandwidth requirements. Now, add the traffic of all the applications and multiply that by the number of users in the workgroup, the department, the floor, and the wiring closet. Thus there is an ever increasing requirement for processing speed as well as bandwidth and the demand for Gigabit Ethernet has been intensifying.

1.2 The OSI Reference Model

Network models are structured into layers, with each layer representing a specific networking function. These functions are controlled by protocols, which are rules that govern end-to-end communication between devices. The Open Systems Interconnection (OSI) model was developed by the International Organization for Standardization (ISO), and formalized in 1984. It provided the first framework governing how information should be sent across a network. It gives a platform for a common technical language and has led to the standardization of communications protocols and the functions of a protocol layer. The structure and functions of the OSI architecture is given in the Figure 1.2.1 [3].

User Application Programs

RESPONSIBILITY OF HOST SYSTEM	Layer 7	Application	Provides general services related to application (e.g. file transfer, user access)	SUPPORT USER APPLICATIONS
	Layer 6	Presentation	Formats data (Encodes, encrypts, compresses)	
	Layer 5	Session	Maintains dialog between communication devices	
	Layer 4	Transport	Provides reliable end-to-end data transmission	
RESPONSIBILITY OF NETWORK	Layer 3	Network	Switches and routes information units	GOVERNS THE COMMUNICATION FACILITIES
	Layer 2	Data Link	Provides data exchange between devices on the medium	
	Layer 1	Physical	Transmits bit stream to physical medium	

Figure 1.2.1 Structure and functions of the OSI architecture

The services provided by each Protocol Layer is summarized below: [4,5].

Physical Layer

The physical layer is the lowest layer of the OSI model. It deals with the transmission and reception of the raw bit stream over a physical medium. It describes the mechanical and electrical or optical specifications and functional interfaces to the transmission medium, and carries the signals for all of the higher layers. It provides data encoding, physical medium attachment, transmission technique, physical medium transmission, data rate, synchronization of bits, line configuration, physical topology and transmission mode.

Data Link Layer

The data link layer provides error-free transmission of data frames from one node to another over the physical layer It allows the above layers to assume virtually error-free transmission over the link. It provides link establishment and termination, Physical addressing, Frame traffic control, Frame sequencing, Frame acknowledgment, Detects and recovers from errors that occur in the physical layer, Frame delimiting, Frame error checking and Media access management. The data link layer is partitioned into the Logical Link Control (LLC) and the media access control(MAC) sublayers. The LLC is common to all LANs and handles functions such as connection setup, initialization, data formatting, address recognition, error control, flow control and connection termination. Thus this sublayer supervises the transmission of a packet between nodes. The MAC layer handles access to the shared medium and is specific to the type of LAN that is implemented.

Network Layer

The network layer deals with the delivery of packets from source-to-destination, possibly across multiple links. It provides routing, Subnet traffic control, Frame fragmentation, Logical-physical address mapping, Subnet usage accounting.

Transport Layer

The transport layer ensures that the data frames delivered are error-free, in sequence, and there are no losses or duplications. The higher layer protocols need not be concerned with the transfer of data between them and their peers. The type of service that is obtained from the network layer determines the size and complexity of a transport protocol. A minimal transport layer is required for a reliable network layer with virtual circuit capability. The transport protocol should include extensive error detection and recovery for unreliable network layers. The transport layer provides message segmentation, message acknowledgment, message traffic control and session multiplexing.

Session Layer

The session layer is responsible for session establishment between different communicating stations. It provides, session establishment, maintenance and termination and session support.

Presentation Layer

The presentation layer deals with the syntax and semantics of the information exchanged. It formats the data to be presented to the application layer and can be viewed as the translator for the network. The presentation layer provides, character code translation, data conversion, data compression and data encryption.

Application Layer

The application layer enables the users and application processes to access the network. It provides functions such as resource sharing, remote file access, remote printer access, inter-process communication, network management, directory services, electronic messaging and network virtual terminals.

1.3 TCP/IP Protocol suite

Transmission Control Protocol/Internet Protocol (TCP/IP) is a hierarchical protocol suite, [5] made up of interactive modules. Each module provides a specific functionality and the modules may not be interdependent. The layers of the TCP/IP Protocol suite contain relatively independent protocols that can be mixed and matched depending on the needs of the system. Figure 1.3.1 gives a comparison of TCP/IP and OSI models.

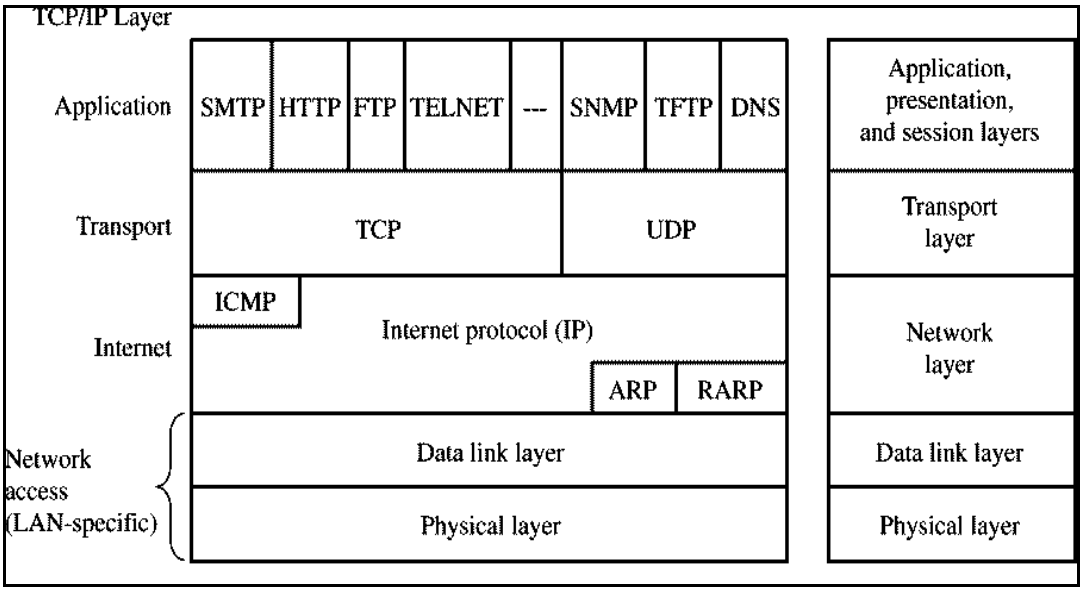

Figure 1.3.1 Comparison of TCP/IP and OSI models [3]

1.4 IEEE Project 802

The Working Group 802 of the IEEE has been a major creator of specifications for Local Area Network (LAN) architectures. The IEEE-802 LAN standards are modularly structured and consist of a powerful set of protocols. The LAN management functions are subdivided into those that can be generalized and those that must remain specific to a particular LAN architecture.

Figure 1.4.1 illustrates the IEEE-802 LAN Model and compares it with OSI model [3].

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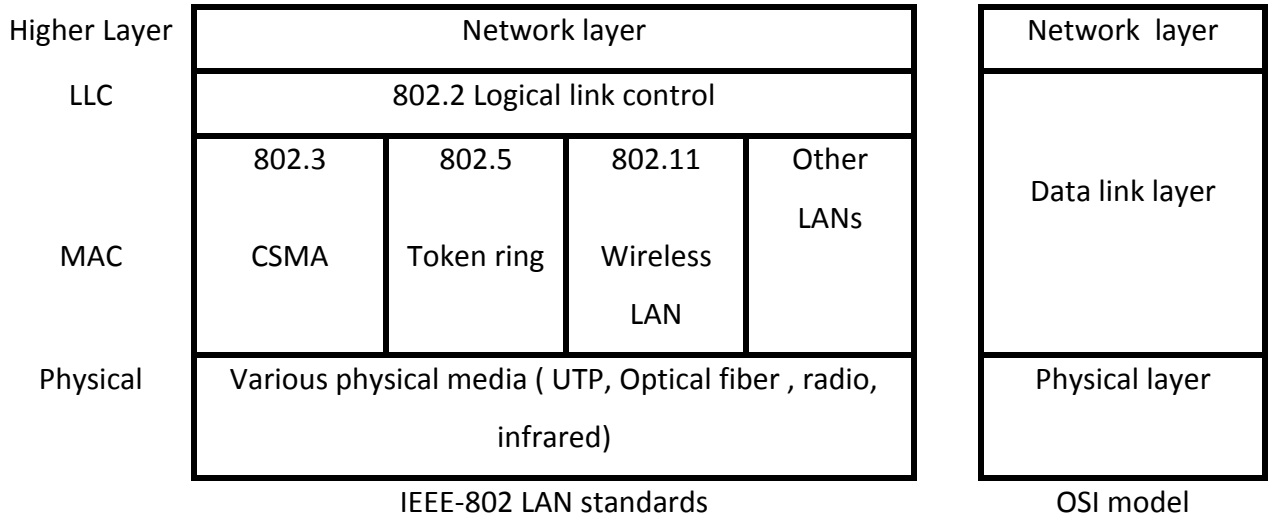

Figure 1.4.1 The IEEE-802 LAN Model

The IEEE 802 LAN/MAN (Metropolitan Area Network) Standards Committee develops and maintains networking standards and recommended practices for local, metropolitan, and other area networks, using an open and accredited process, and advocates them on a global basis. The most extensively used standards are for Ethernet, Bridging and Virtual Bridged LANs, Wireless LAN, Wireless Personal Area Network (PAN), Wireless MAN, Wireless Coexistence, Media Independent Handover Services, and Wireless Rural Area Network (RAN) [6].

Following is the list of various IEEE-802 subgroups and technical advisory groups (TAG):

IEEE 802 Working Groups and Study Groups

- 802.1 Higher Layer LAN Protocols Working Group
- 802.3 Ethernet Working Group
- 802.11 Wireless LAN Working Group
- 802.15 Wireless Personal Area Network (WPAN) Working Group

- 802.16 Broadband Wireless Access Working Group
- 802.18 Radio Regulatory TAG
- 802.19 Wireless Coexistence Working Group
- 802.21 Media Independent Handover Services Working Group
- 802.22 Wireless Regional Area Networks
- 802.24 Smart Grid TAG
- OmniRAN EC Study Group

Hibernating Working Groups

- 802.17 Resilient Packet Ring Working Group
- 802.20 Mobile Broadband Wireless Access (MBWA) Working Group

Disbanded Working Groups and Study Groups

- 802.2 Logical Link Control Working Group
- 802.4 Token Bus Working Group (material no longer available on this web site)
- 802.5 Token Ring Working Group
- 802.6 Metropolitan Area Network Working Group (material no longer available on this web site)
- 802.7 Broadband TAG (material no longer available on this web site)
- 802.8 Fiber Optic TAG (material no longer available on this web site)
- 802.9 Integrated Services LAN Working Group (material no longer available on this web site)
- 802.10 Security Working Group (material no longer available on this web site)
- 802.12 Demand Priority Working Group (material no longer available on this web site)
- 802.14 Cable Modem Working Group (material no longer available on this web site)
- 802.23 Emergency Services Working Group
- QOS/FC Executive Committee Study Group (material no longer available on this web site)

- ECSG TVWS TV Whitespace study group
- ES-ECSG Emergency Services Executive Committee Study Group

IEEE 802.3 Ethernet Working Group

List of active projects, study groups, and ad hocs as listed below:

- IEEE P802.3bj 100 Gb/s Backplane and Copper Cable Task Force.
- IEEE P802.3bm 40 Gb/s and 100 Gb/s Fibre Optic Task Force.
- IEEE P802.3bn EPON Protocol over Coax (EPoC) Task Force.
- IEEE P802.3bp Reduced Twisted Pair Gigabit Ethernet PHY Task Force.
- IEEE P802.3bq 40GBASE-T Task Force.
- IEEE P802.3br Interspersing Express Traffic Task Force.
- IEEE P802.3bt DTE Power via MDI over 4-Pair Task Force.
- IEEE P802.3bu 1-Pair Power over Data Lines (PoDL) Task Force.
- IEEE 802.3 400 Gb/s Ethernet Study Group.
- IEEE 802.3 Industry Connections NG-EPON Ad Hoc.

Archive information of completed work:

- IEEE Std 1802.3-2001Conformance test reaffirmation.
- IEEE 802.3 Trunking Study Group.
- IEEE 802.3 Higher Speed Study Group.
- IEEE 802.3 DTE Power via MDI Study Group.
- IEEE 802.3 10GBASE-CX4 Study Group.
- IEEE 802.3 10GBASE-T Study Group.
- IEEE 802.3 Backplane Ethernet Study Group.
- IEEE 802.3 10 Gb/s on FDDI-grade MM fiber Study Group.
- IEEE 802.3 Power over Ethernet Plus Study Group.
- IEEE 802.3 Residential Ethernet Study Group.

- IEEE 802.3 Energy Efficient Ethernet Study Group.
- IEEE 802.3 Higher Speed Study Group.
- IEEE 802.3 100 Gb/s Backplane and Copper Study Group.
- IEEE 802.3 Extended EPON Study Group.
- IEEE 802.3 Next Generation 40 Gb/s and 100 Gb/s Optical Ethernet Study Group.
- IEEE 802.3 EPON Protocol over a Coax (EPoC) PHY Study Group.
- IEEE 802.3 Reduced Twisted Pair Gigabit Ethernet (RTPGE) Study Group.
- IEEE 802.3 Next Generation BASE-T Study Group.
- IEEE 802.3 Distinguished Minimum Latency Traffic in a Converged Traffic Environment Study Group.
- IEEE 802.3 4-Pair Power over Ethernet (PoE) Study Group.
- IEEE 802.3 1-Pair Power over Data Lines (PoDL) Study Group.
- IEEE Std 802.3z-1998, Gigabit Ethernet.
- IEEE Std 802.3aa-1998, Maintenance #5.
- IEEE Std 802.3ab-1999, 1000BASE-T.
- IEEE Std 802.3ac-1998, VLAN TAG.
- IEEE Std 802.3ad-2000, Link Aggregation.
- IEEE Std 802.3ae-2002, 10 Gb/s Ethernet.
- IEEE Std 802.3af-2003, DTE Power via MDI.
- IEEE Std 802.3ag-2002, Maintenance #6 (Revision).
- IEEE Std 802.3ah-2004, Ethernet in the First Mile.
- IEEE Std 802.3aj-2003, Maintenance #7.
- IEEE Std 802.3ak-2004, 10GBASE-CX4.
- IEEE Std 802.3REVam-2005, Maintenance #8 (Revision).
- IEEE Std 802.3an-2006, 10GBASE-T.
- IEEE Std 802.3ap-2007, Backplane Ethernet.
- IEEE Std 802.3aq-2006, 10GBASE-LRM.
- IEEE P802.3ar, Congestion Management.
- IEEE Std 802.3as-2006, Frame Expansion.

- IEEE Std 802.3at-2009, DTE Power Enhancements.
- IEEE Std 802.3-2005/Cor 1-2006 (IEEE 802.3au) DTE Power Isolation Corrigendum.
- IEEE Std 802.3av-2009, 10 Gb/s PHY for EPON.
- IEEE Std 802.3-2005/Cor 2-2007 (IEEE 802.3aw), 10GBASE-T Corrigendum.
- IEEE Std 802.1AX-2008 (IEEE 802.3ax), Link Aggregation.
- IEEE Std 802.3-2008 (IEEE 802.3ay), Maintenance #9 (Revision).
- IEEE Std 802.3az-2010, Energy-efficient Ethernet.
- IEEE Std 802.3ba-2010, 40 Gb/s and 100 Gb/s Ethernet.
- IEEE Std 802.3-2008/Cor 1-2009 (IEEE 802.3bb) Pause Reaction Delay Corrigendum.
- IEEE Std 802.3bc-2009 Ethernet Organizationally Specific type, length, values (TLVs).
- IEEE Std 802.3bd-2011 MAC Control Frame for Priority-based Flow Control.
- IEEE Std 802.3.1-2011 (IEEE 802.3be) Ethernet MIBs .
- IEEE Std 802.3bf-2011 Ethernet Support for the IEEE P802.1AS Time Synchronization Protocol.
- IEEE Std 802.3bg-2011 40Gb/s Ethernet Single-mode Fibre PMD.
- IEEE Std 802.3-2012 (IEEE 802.3bh) Revision to IEEE Std 802.3-2008.
- IEEE Std 1802.3-2001, Conformance Test Maintenance #1.
- IEEE Std 802.3.1-2013 (IEEE 802.3.1a) Revision to IEEE Std 802.3.1-2011 Ethernet MIBs.
- IEEE Std 802.3bk-2013 Extended EPON.
- IEEE P802.3 Ethernet over LAPS liaison Ad hoc.
- IEEE P802.3 Static Discharge in Copper Cables Ad hoc.
- IEEE P802.3 100BASE-FX over dual Single Mode Fibre Call For Interest.

1.5 History of Ethernet

The University of Hawaii's ALOHA network is considered to be the ancestor of all shared media networks[7]. In 1968, Norman Abramson developed a packet radio networking system that ran at 4800bps and 9600bps. In 1973, Robert Metcalfe and David Boggs at Xerox Corporation in Palo Alto, CA applied the ALOHA network principles and created the world's first

LAN illustrated in Figure 1.5.1. The network was first named as ALTO ALOHA and later changed to Ethernet. This first version of Ethernet had a speed upto 2.94 Mbps.

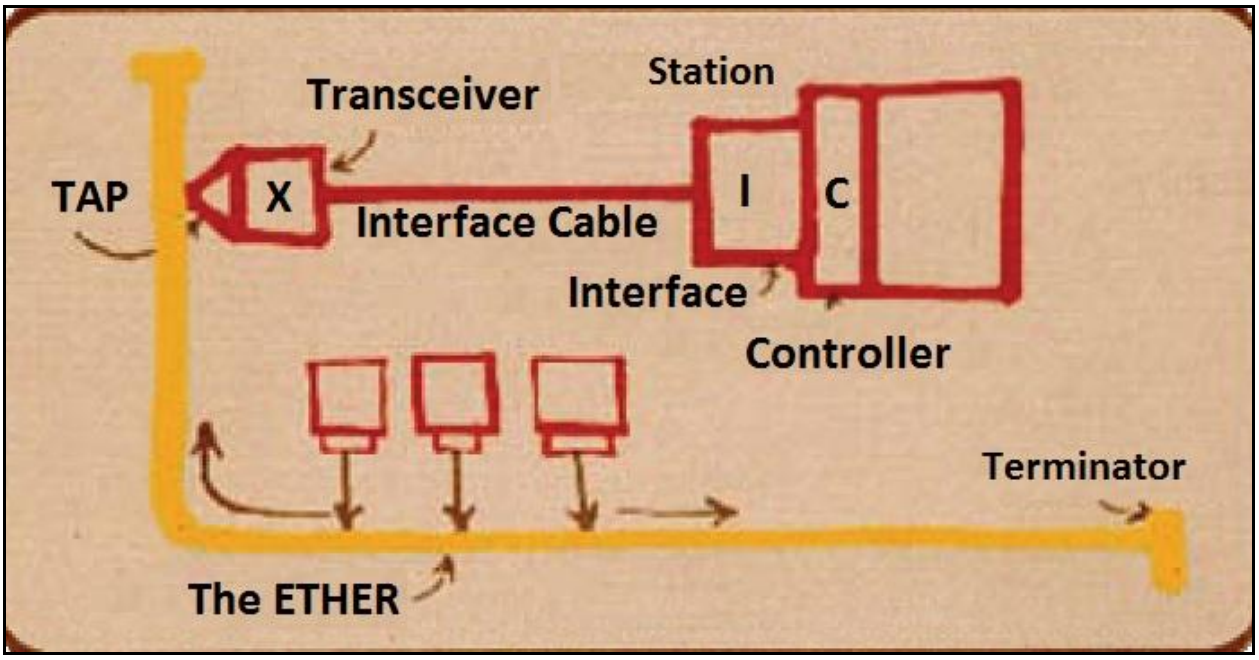

Figure 1.5.1 World's first LAN [8]

This version was used by the White House for word processing. However, this version of Ethernet was not successfully commercialized. The first commercial version of Ethernet was released by DEC, Intel, and Xerox (DIX) in 1980. It was known as Ethernet DIX 80. The second revision release, Ethernet, Version2, Ethernet DIX 82, was released in 1982, which is the standard of Ethernet technology that is in use today. The IEEE formed Project 802 to provide a framework for the standardization of LAN technology. Novell released Novell Netware'86 in 1983, that used a proprietary frame format based on a preliminary specification of the IEEE 802.3 standard. Novell software is used to manage printers and servers.

In 1983, the IEEE approved the IEEE 802.3 standard, which included IEEE 802.2 LLC. This made Novell Netware's proprietary format incompatible with the latest technology. This incompatibility was resolved by creating Sub-Network Access Protocol (SNAP) for the new IEEE 802.3 standard. The overall packet specifications were finalized and then the transmission

medium needed to be agreed upon. In the late 1980s, SynOptics Communications defined and developed a mechanism for transmitting 10Mbps Ethernet signals over twisted-pair cables. Thus, the amalgamation of a low cost transmission medium with agreed packet technology specifications heralded the wide deployment of Ethernet. The Ethernet-over-twisted-pair specification (10BASE-T) was approved by the IEEE in 1990 as the IEEE802.3i standard. It rapidly became the ideal Ethernet media type. Following Figure 1.5.2 summarizes the timeline of Ethernet evolution upto 10Gbps.

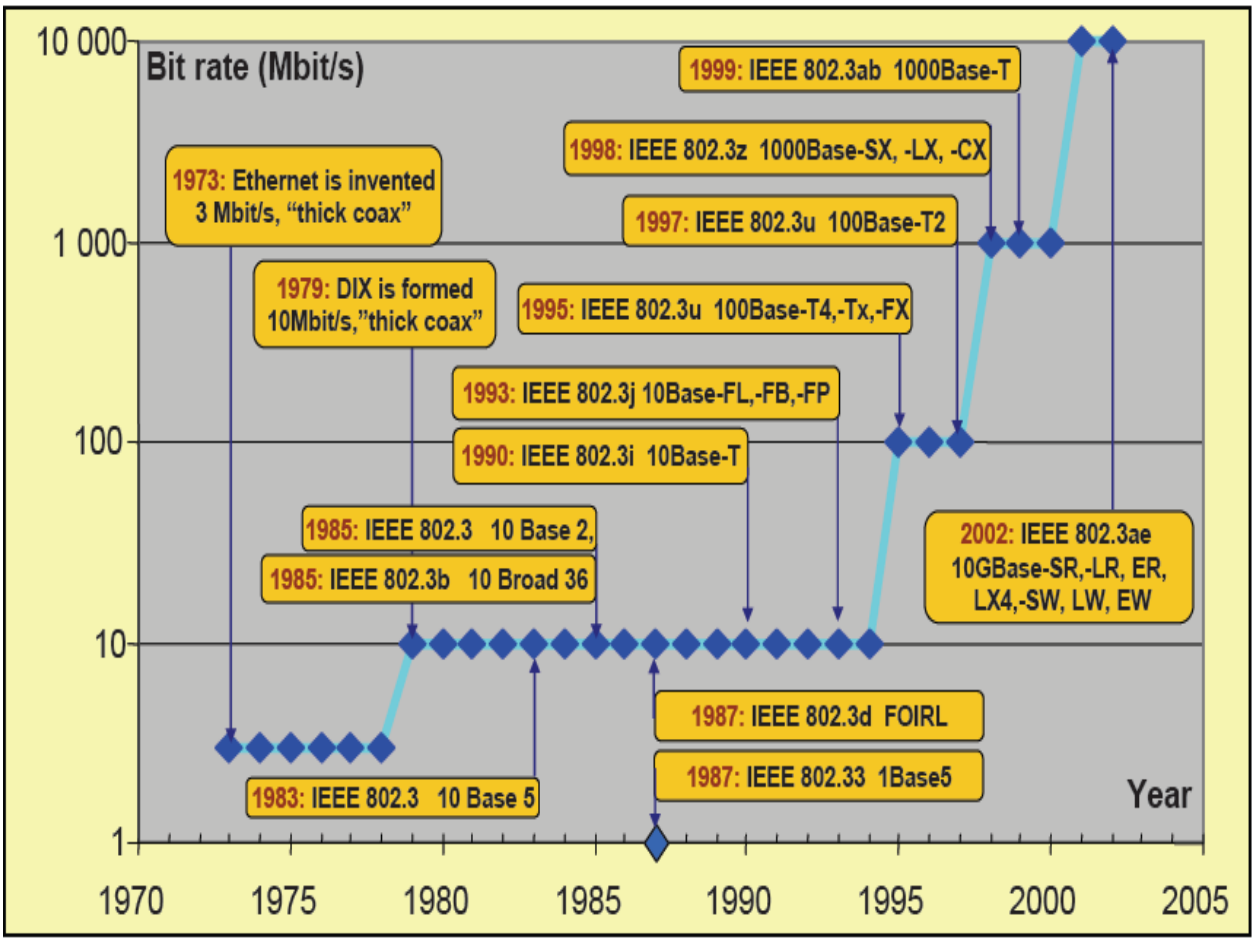

Figure 1.5.2 Timeline of Ethernet evolution [9]

10 Mbps Ethernet evolved to Fast Ethernet (100 Mbps), then Gigabit Ethernet (1000 Mbps), 10 Gigabit Ethernet (10,000 Mbps) and recently to 100Gbps and 400Gbps [144].

Ethernet has evolved rapidly over the past three decades, however, the basic Ethernet frame format and principles of operation have remained practically unaltered. As a result, networks of diverse speeds (10/100/1000 Mbps) operate uniformly without the need for packet fragmentation, packet reassembly or address translation. The advancements in Ethernet have mainly focused on speed and affordability of related cabling and transceiver technologies. It has moved from coax to twisted pair and fiber optic cables and also has been the basis for advanced wireless technologies as IEEE 802.11 Wireless Local Area Network(WLAN) and IEEE 802.16 Worldwide Interoperability For Microwave Access (WiMAX) [10] . As a result, every packet in today's networks starts and ends its existence as Ethernet. Even The next generation of cellular networks will also use this simple, ubiquitous, and extensible technology. Table 1.5.1 gives the Evolution of Ethernet from 10 Mbps to 400Gbps.

Table 1.5.1 Evolution of Ethernet Standards from 10 Mbps to 400Gbps[11].

The Evolution of Ethernet Standards				
Date	**IEEE Standards**	**Name**	**Data Rate**	**Type of cabling**
1990	802.3i	10BASE-T	10Mbps	Cat-3
1995	802.3u	100BASE-TX	100Mbps	Cat-5
1998	802.3z	1000BASE-SX	1Gbps	Multimode fiber
	802.3z	1000BASE-LX/EX		Single mode fiber
1999	802.3ab	1000BASE-T	1Gbps	Cat- 5e or higher
2003	802.3ae	10GBASE-SR	10Gbps	Laser optimized MMF
	802.3ae	10GBASE-LR/ER		Single mode fiber
2006	802.3an	10GBASE-T	10Gbps	Cat-6A
2015*	802.3bq	40GBASE-T	40Gbps	Cat-8 (Class I & II)
2010	802.3ba	40GBASE-SR4/LR4	40Gbps	Laser optimized MMF or SMF
2015*	802.3ba	100GBASE-SR10/LR4/ER4	100Gbps	Laser optimized MMF or SMF
	802.3bm	100GBASE-SR4	100Gbps	Laser optimized MMF

2016*	802.3bs	Under development	400Gbps	Laser optimized MMF or SMF
Note : *These are the proposed study groups				

1.6 Gigabit Ethernet

Gigabit Ethernet has been designed to adhere to the standard Ethernet frame format and maintains compatibility with the installed base of Ethernet and Fast Ethernet products. Thus there is no requirement of frame translation. Figure 1.6.1 describes the IEEE 802.3 Ethernet frame format.

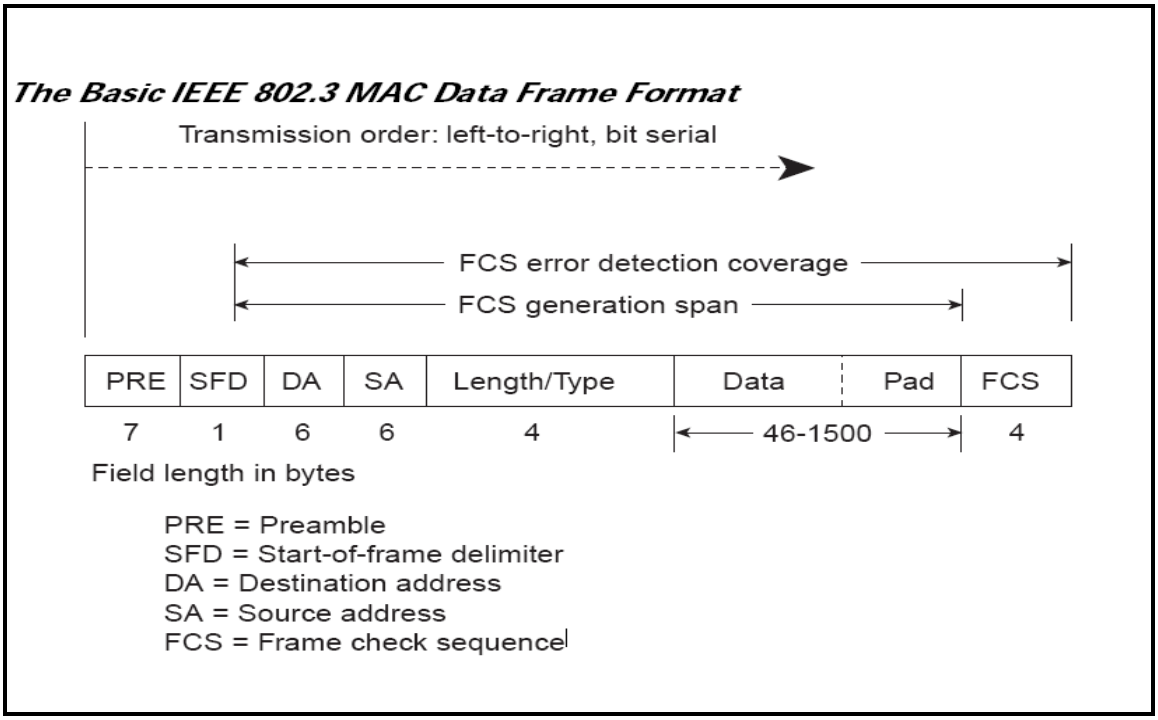

Figure 1.6.1 IEEE 802.3 Ethernet Frame Format [12]

The strategy for Gigabit Ethernet is the same as that for 100-Mbps Ethernet. It defines a new medium and transmission specification, but retains the carrier sense multiple access collision detect (CSMA/CD) protocol and frame format of its 10- and 100-Mbps predecessors [13]. Thus, it maintains compatibility with the slower Ethernet standards, providing a smooth

migration path. Figure 1.6.2 shows a distinctive application of Gigabit Ethernet [14] . A 1-Gbps LAN switch provides backbone connectivity for central servers and high-speed workgroup switches. Each workgroup LAN switch supports both 1-Gbps links, to connect to the backbone LAN switch and also supports high-performance workgroup servers, and 100-Mbps links. Thus high-performance workstations, servers, and 100-Mbps LAN switches are consistently supported.

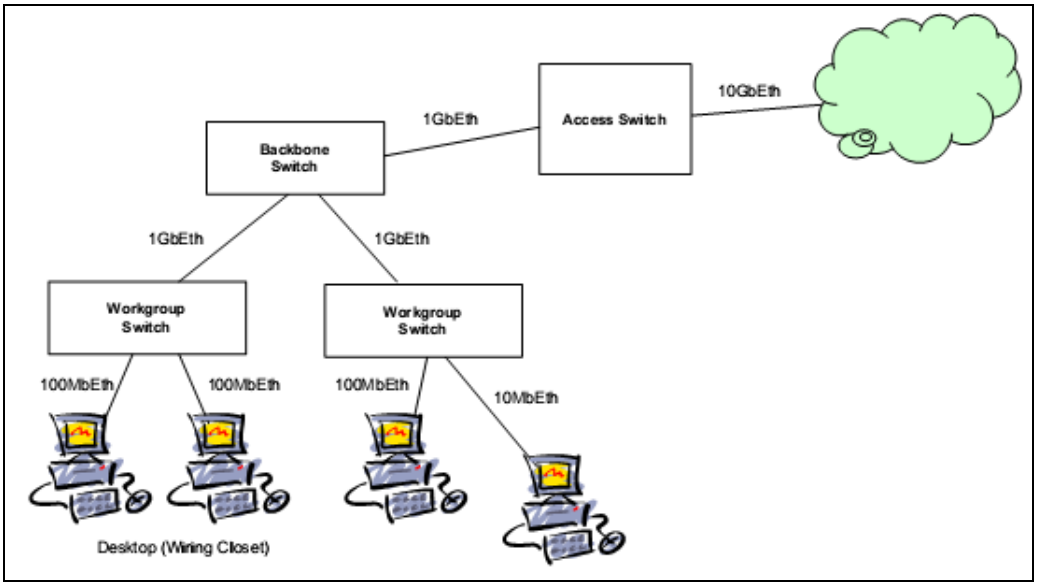

Figure 1.6.2 Enterprise LAN Topology [14]

Gigabit Ethernet Protocol Architecture

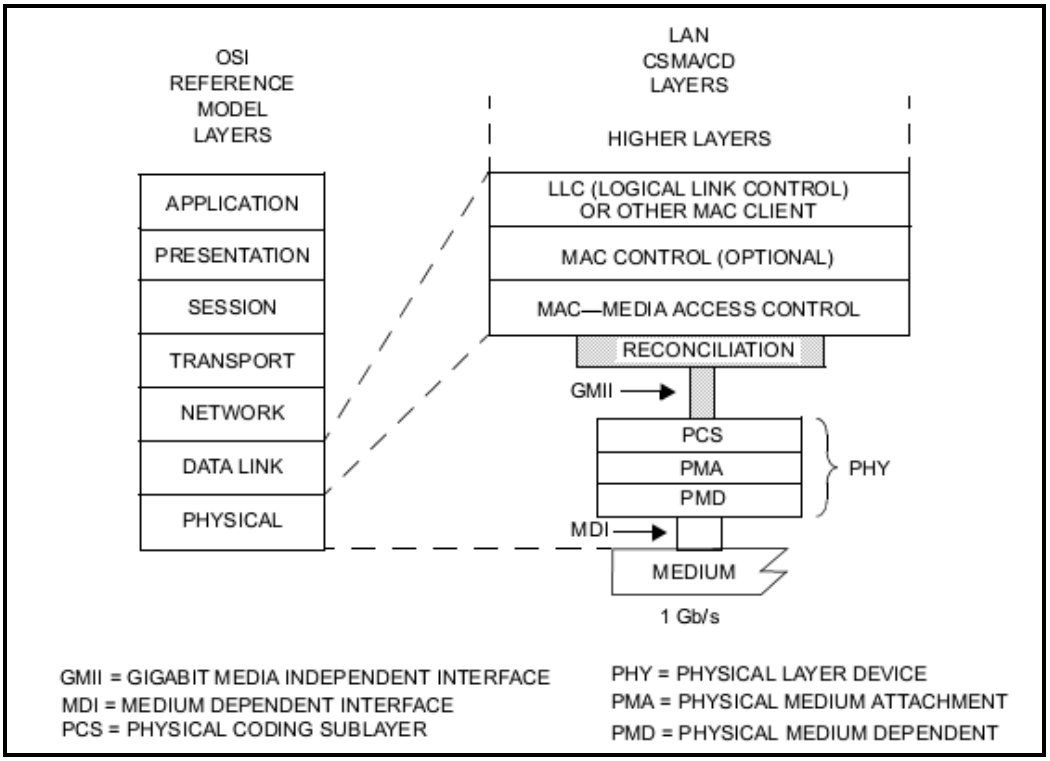

Figure 1.6.3 Gigabit Ethernet protocol architecture [12]

The various layers of the Gigabit Ethernet protocol architecture are shown in Figure 1.6.3. The GMII (Gigabit Media Independent Interface) is the interface between the MAC layer and the Physical layer. It allows any physical layer to connect with the MAC layer and is an extension of the Media Independent Interface (MII) used in Fast Ethernet. The management interface is the same as MII. It supports 10, 100 and 1000 Mbps data rates and provides separate 8-bit wide receive and transmit data paths. Thus, it supports both full-duplex as well as half-duplex operation.

The GMII has 2 media status signals : one indicates presence of the carrier, and the other indicates absence of collision. The Reconciliation Sublayer (RS) maps these signals to Physical Signalling (PLS) primitives which is understood by the MAC sublayer. The same MAC controller can be used with various media types such as shielded and unshielded twisted pair cable, single-mode and multi-mode optical fibre.

The GMII is divided into three sublayers :

Physical Coding Sublayer (PCS)

It provides a uniform interface to the Reconciliation layer for all physical media. It uses 8B/10B coding like Fibre Channel, whereby groups of 8 bits are represented by 10 bit "code groups". Some code groups represent 8 bit data symbols and others represent control symbols. Control symbols are used in Carrier Extension. It generates indications for Carrier Sense and Collision Detection and also manages the auto-negotiation process which is used to determine the network speed (10,100 or 1000 Mbps) and mode of operation (half-duplex or full-duplex).

Physical Medium Attachment (PMA)

This sublayer enables a medium-independent means for the PCS to support various serial bit-oriented physical media. This layer serializes code groups before transmission and deserializes bits received from the medium into code groups.

Physical Medium Dependent (PMD)

This sublayer maps the physical medium to the PCS and defines the physical layer signalling used for various media. The Medium Dependent Interface (MDI), which is a part of PMD is the actual physical layer interface attachments such as connectors, for different media types.

1.7 Emerging trends in Ethernet technologies

Ethernet has played a dominant role today not only for data centers and high-performance computing systems, but also for desktops and laptops. There were other less used network architectures such as, Token Ring, Fiber Distributed Data Interface (FDDI), Asyncronous Tranfer Mode (ATM), High Performance Parallel Interface (HIPPI) and Myrinet that competed with Ethernet in one or more areas. However, Ethernet has not taken over the whole market for standards-based, data networking. Most server vendors offer options for supporting Fiber Channel for attachment of high-performance storage controllers in storage area

networks, and InfiniBand for tightly coupled cluster computing and some high-end storage applications [15]. These networks provide features and capabilities which are not currently available in Ethernet. Thus, they are likely to find oppurtunities in applications beyond the focus of Ethernet vendors.

Table 1.7.1 gives a detailed specification of the Gigabit Ethernet technologies from 1Gbps to 100Gbps[15]

Ethernet Variant	Data rate (Gbps)	Min. Reach (meters)	Form Factor	Media Wavelenghth	Standard IEEE 802.3
1000BASE-					
T	1	100	RJ45, SFP, GBIC	TP Copper	ab
SX		300	GBIC, SFP	LQMF 850nm	Z
LX		5000	GBIC, SFP	SMF 1310nm	
CX		25	HSSDC/DB9	Twinax Copper	
ZX		70,000	GBIC, SFP	SMF 1550 nm	Defacto
10GBASE-					
Ethernet Variant	Data rate (Gbps)	Min. Reach (meters)	Form Factor	Media Wavelenghth	Standard IEEE 802.3
SR	10	300	XENPAK, XFP, X2, SFP+	LQMF 850nm	
LR		10,000	300-oin, XENPAK, XFP, X2, SFP+	SMF 1310nm	

LX4	4 x 2.5	300	XENPAK, X2	FDDI- grade MMF 1310nm	ae-2002/-2005
ER	10	40,000	XENPAK,XFP, X2	SMF 1550nm	
ZR		80,000	XENPAK, SFP+	SMF 1550nm	
LRM		220	XFP, SFP+	FDDI- grade MMF 1310nm	aq-2006/-2006
CX4		15	MicroGigaCN	Twinax Copper	ak-2004/-2005
T		100	RJ45 CAT6A or above	TP Copper	an-2006/-2006
CR		15	SFP+ Direct Attach Copper	Twinax Copper	SFF standard
40GBASE					
CR4	4 x 10 G	7	QSFP+ Direct attached Copper	Twinax Copper	bg
SR4		100/125	QSFP+	LQMF 850nm	
LR4		10,000	QSFP+, CFP	SMF 1310nm	
FR	40G	2000	CFP	SMF 1310nm/1550nm	bg
100GBASE					
CR10	10 x 10	7	CXP Direct attached Copper	Twinax Copper	ba
SR10		100/125	CXP, CFP	LQMF 850nm	
LR4	4 x 25	10,000	QSFP+, CFP	SMF 1310nm	

ER4		40,000	CFP	SMF 1550nm	
40GBase-					
TBD*	4 x 10	40,000	TBD/QSFP+, CFP2, CFP4	SMF 1550nm	bm
100GBase-					
CR4	4 x 25	Board – TBD Cable – 5m	PHY and Management Parameter for 100 Gbps Operation Over Backplane and copper Cables	Copper	bj
UR4*	4 x 25	20	TBD/QSFP+, CFP2, CFP4		
SR4	4 x 25	100	TBD/QSFP+, CFP2, CFP4	LOMF 850nm	bm
Note : *These are proposed and not yet in the draft standard.					

Deployment of 10 Gb/s Ethernet has followed a much slower adoption following standardization, and much lower total volumes. There may be two likely reasons for this. First, design and standardization of 10 Gb/s links over twisted-pair cable has taken a long time. Hence, more expensive optical transceivers and cables had to be used. Moreover, twisted-pair cabling at 10 Gb/s data rates required PHY circuits with sophisticated signal-processing capability. Within enterprise installations, 100 Gb/s Ethernet will be the dominant technology for interconnecting servers to each other and to storage and high-end parallel visualization systems. The IEEE has announced a new group that aims to bring wired Ethernet speeds up to 1 Tbps by 2015 and as fast as 10 Tbps by 2020. This announcement is based on the publication of the IEEE 802.3 Ethernet Bandwidth Assessment report, which found that terabit-speed networks will be essential to support overall capacity requirements by 2015 if current trends continue [16]. The report found that, in 2010, the majority of IXP (Internet Exchange Provider)

links were running at 10Gbps, while all other forms of Ethernet were trending downward in the industry as shown in Figure 1.7.1.

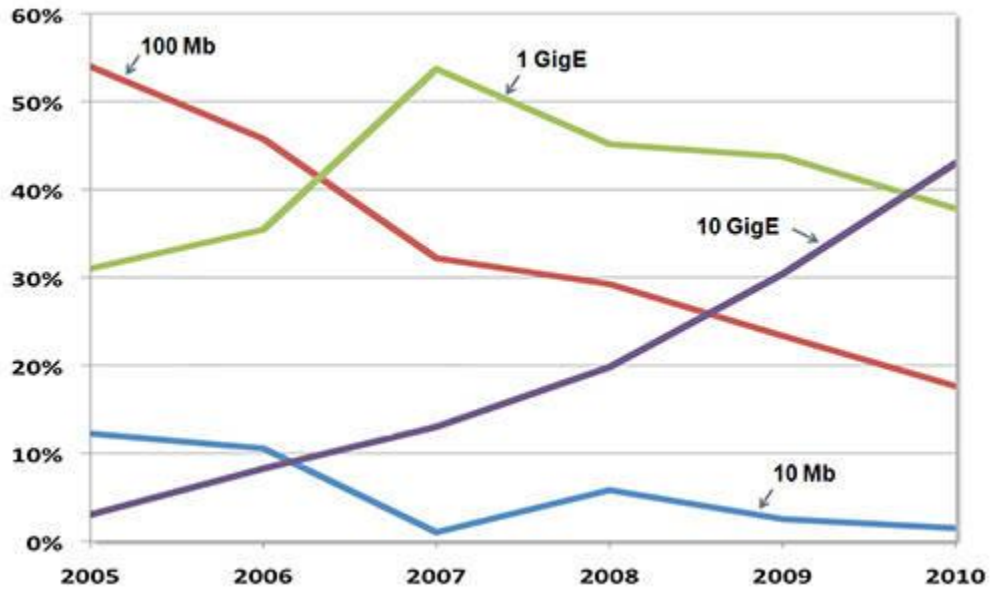

Figure 1.7.1 Use of 10Gbps Ethernet has grown steadily among internet exchange providers [6]

As of 2011, amount of bandwidth used by streaming media had more than doubled since the previous year. The most aggressive growth in network bandwidth utilization is in the financial sector and in High Performance Computing (HPC) for data-intensive science, the IEEE report found. For example, the Large Hadron Collider pushes 15 petabytes of data per year to Tier 1 storage sites around the world. Also, the high-frequency trading systems used by the finance industry, transmit data uncompressed, hence resulting in larger bandwidth consumption. Figure 1.7.2 projects the dominating Gigabit Ethernet links in 2011 and 2013.

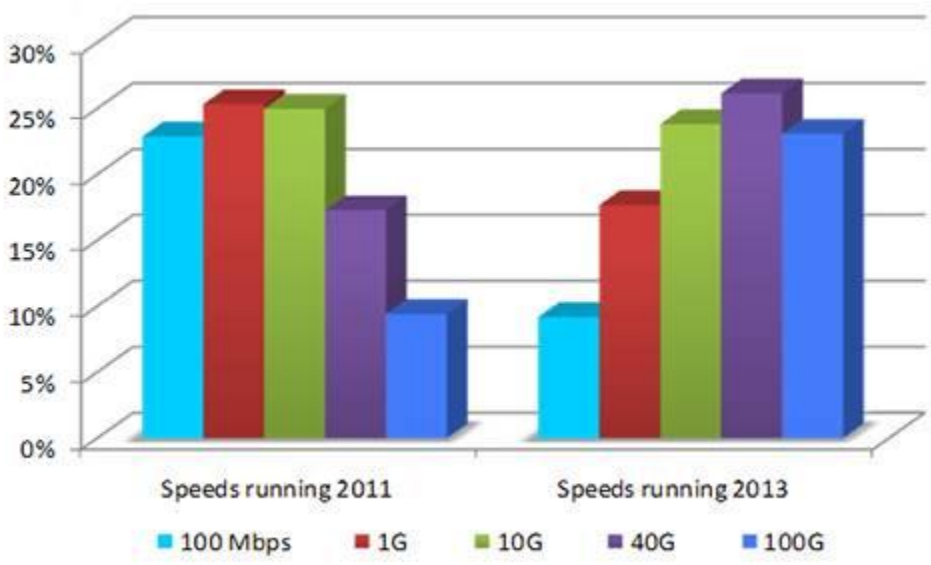

Figure 1.7.2 Dominating Gigabit Ethernet links [6]

A recent study by Intel has concluded that the Ethernet protocol is now on more than 90 percent of all networked devices globally. That percentage will grow as the "Internet of things" allows an enormous number of devices to communicate with each other and with us [17]. Figure 1.7.3 illustrates the impact of 100 Gbps Ethernet.

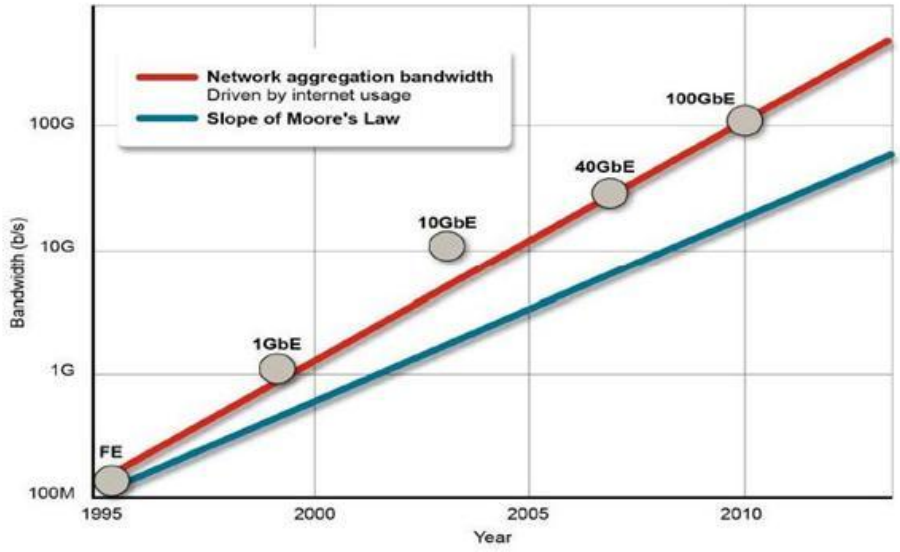

Figure 1.7.3 Impact of the 100Gbps Ethernet [18]

Even while the standards committees are debating the implementation of 400 Gbps standard for Ethernet, Metcalfe noted that it's time to start thinking about terabit Ethernet, probably with a 64-bit addressing system. Considering the rate of innovation that Ethernet seems to spawn, looks like Terabit Ethernet will appear in 10 years or less.

1.8 Literature Review

The scope of research can be broadly classified into three main categories namely the performance analysis of Gigabit Ethernet protocol, the development of Cyclic Redundancy Check (CRC) algorithms for error detection and their performance studies and the study of error correction codes used in noisy communication channels. Hence, we give a brief literature review of the areas of interest as follows:

1.8.1 Review of Performance Analysis of Gigabit Ethernet

Performance analysis of Gigabit Ethernet standard 802.3z Gigabit Ethernet was made on a simulated network with different number of stations and packet sizes by S. Finkler and D. Sidhu [19]. Gigabit Ethernet is able to maintain a throughput of 60-80% for packet sizes less than slotTime and maintains 90-98% throughput for larger packet sizes. Because of bursting, it scales very well for a large number of transmitting stations. Various experiments and analysis were carried out and Gigabit Ethernet maintained a throughput greater than 90% for upto 200 stations.

Design and evaluation of the hardware platform for the Field Programmable Gate Array (FPGA)-based Gigabit Ethernet/PCI Network Interface Card (NIC) using Avnet platform and Xilinx MAC core was studied extensively by Tinoosh M. [20] at Houston, Texas in 2004. The FPGA-based NIC uses multiple memories, including SDRAM SODIMM, for adding different network services. Experimental results at Gigabit Ethernet receive interface reveal that the NIC can receive all packet sizes and store them at SDRAM at Gigabit Ethernet line rate. The overall throughput, transfer latency and bus utilization is improved by improving the processing latency of each interface. The receive FIFO provides enough buffering space for up to 10

incoming large frames of 1518 bytes, thus improving the performance in receiving small packets. The latency in bus interface operations is reduced by pipelining and improving the RTL coding in OPB interface implementations, which results in 32% reduction in total data transfer latency and 72.5% improvement throughput for OPB single transfers.

A partially reconfigurable network controller IIM7010 was developed on a Xilinx Virtex-II XCV1000 FPGA in [21]. The functioning of this controller was then verified and also its throughput and packet loss was analysed. Tests were conducted to find the impact of partial reconfiguration on the performance of network controllers. IIM7010 network controller uses the TCP/IP family of protocols to communicate over a 10 Mbps Ethernet LAN network.

The Gigabit Ethernet platform based on a PCI card was designed and built at CERN, Geneva, Switzerland in 2005 [22]. Altera Stratix FPGA was the main component. Two Gigabit Ethernet applications were implemented, namely a network tester and a network emulator. The network tester was used to assess network equipment intended to be used in the ATLAS TDAQ network. It is used to verify whether all switching devices meet the required specifications. The network emulator is a packet processor, whose architecture comprises a packet path and a control path. It can introduce a quality degrader and the behaviour of an application can be studied under different types of network conditions.

The design of NIC using Altera Stratix II GX was discussed by Bianco [23], which uses about 33% of the 41,250 logic elements of the FPGA. The developed NICs were incorporated on a high-end PC with a SuperMicro X5DPE-G2 mainboard with one 2.8GHz Intel Xeon processor, 1 Gbyte of PC1600 DDR RAM comprising of two interleaved banks, achieving the memory bus transfer rate up to 3.2 Gbyte/s. The motherboard consists of three PCI-X 133 and three PCI-X 100 slots having peak transfer rates of 1 Gbyte/s and 0.8 Gbyte/s respectively. The board used as NIC is equipped with an Altera Stratix GX FPGA. The FPGA consists of 3 Mbit of integrated DRAM, which can be used to allocate FIFOs, buffers and storage of debug data. All queues are about 15 kbytes. The PCI core supports all frequencies of the PCI-X standard. The scheduling algorithm and the manipulation of packets can use maximum clock frequency of 66MHz. An

Agilent N2X RouterTester 900 with 8 Gigabit Ethernet ports, which could transmit and receive Ethernet frames of any size at full rate, was used as traffic source and sink. This NIC obtained a wire speed data transfer reaching up to 6 Gbit/s of aggregate throughput for 64-byte packets. This work was done in the framework of the EURO project and partly funded by the Italian Ministry of University, Education, and Research.

A reconfigurable and programmable Gigabit Ethernet network interface card RiceNIC was built upon the commercial Avnet Virtex-II Pro development card and provides a custom FPGA design, and all its raw components can function as a system. The NIC includes multiple FPGAs, two 300 MHz embedded PowerPC processors, large on-NIC memories greater than 256 MB, and a copper Gigabit Ethernet interface. Custom NIC firmware is available along with a Linux device driver. RiceNIC can saturate the Gigabit Ethernet network link with maximum-sized packets using a single PowerPC processor. This leaves significant resources on RiceNIC to use for experimental networking research [24].

A new 1-cycle pipeline microprocessor, a fast Ethernet transceiver and low cost high performance embedded network controller was established on Altera Stratix EP1S25F780C6 in [25]. TCP/IP stack is designed to access the Internet. Simulations were performed, where the throughput of Ethernet, UDP (User Datagram Protocol) and TCP packets were found to be 7 Mbps, 5.8 Mbps, and 3.4 Mbps respectively.

An attempt to design Ethernet MAC was made at Dr. M.G.R. University, Chennai, India by D. Thomas and K. S. M. Panicker. They added data compression/decompression to get the data rate more than 1Gbps. In this paper, they argue that it is time to review the MAC layer and incorporate advances made in the protocol performance field during the last twenty years [26].

Gigabit Ethernet data streams were generated over both fibre and copper links using a Xilinx Virtex 4 development system [27]. The paper presents details of the firmware developed to drive the links. Request-response protocols are used and throughput, network latency and packet loss is measured over standard Ethernet networks to PCs. Sequential request and group request DAQ data collection protocols have been implemented. The Virtex4 FPGA contains the hardware embedded MAC modules, which can be combined with the high-speed serial

communication module RocketIO to provide a complete gigabit Ethernet solution without the need for any external support logic. The only hardware required is a standard Small Form-factor Pluggable (SFP) module.

The NetFPGA platform containing Xilinx Virtex2-Pro 50 and Xilinx Spartan II FPGA, which can be programmed with user-defined logic was developed at Stanford University [28]. NetFPGA platform enables rapid prototype and development of multi-Gigabit/second line rate networking applications. The open-source gateware, hardware and software is available. A network traffic capture system and a packet generator was implemented on the NetFPGA. The NetFPGA enables rapid development of hardware-accelerated packet processing applications. The Internet packets can be transmitted at line rate on upto four Gigabit Ethernet ports simultaneously.

IP based Gigabit Ethernet connection is designed and implemented directly in hardware by Nicholas Tsakiris and Greg Knowles in [29]. It implements the ICMP, UDP and the new UDP-Lite standards. It was designed in VHDL and uses 1000 slices of the Xilinx Spartan 3 FPGA, running at full Gigabit ethernet speed.

The Gigabit network performance tester with full line rate is developed using Samsung's S3C2410 processor in [1]. The instrument can measure the performance of network across the sub-network at full line rate. Broadcom's product BCM5421S, supporting 10/100/1000 Mbps speed is used as Ethernet physical layer transceiver.

1.8.2 Review of CRC Error Detection Algorithm Development

Hardware implementation of CRC using LFSR is explained as well as five software algorithms namely Bitwise, On-the-fly, Table Lookup, Reduced Table Lookup, Bytewise and Wordwise Reduced Table Lookup Algorithms are explained along with their codes in [30]. The different algorithms are compared in terms of their speed and storage requirements.

G. Albertango and R. Sisto have presented a method of designing hardware parallel encoders for CRCs which is based on digital system theory and z-transforms in [31]. This method can be used by designers in deriving the logic equations of the parallel encoder circuit

for any generator polynomial. Pei and Zukowski investigate the use of VLSI(Very Lage Scale Integrated Circuit) technology to increase the speed of CRC circuits in [32]. It is found that CMOS technologies can achieve a speed of 1 Gb/s data rates.

Castagnoli et al. have investigated several classes of CRC codes with 24 and 32 parity bits in [33] using the method developed by T. Fujiwara et al. for computing the minimum distance of shortened Hamming codes using the weight distribution of their dual codes. The paper [34] presents the VLSI layout generation of a programmable CRC chip for 16 bit CRC using serial implementation. The chip is simulated at 600MHz speed.

A comparative study of ten different implementation strategies for computation of Cyclic Redundancy Checks has been done in [35].The paper also presents a novel architecture suitable for use as an IP in a protocol processor. The different implementation techniques have been divided into application areas based on their speed, flexibility and power-consumption.

Byte-oriented method for CRC computation is described in [36], which reduces the calculation time by a factor of four. A systematic method to calculate CRC in parallel is introduced in [37]. Galois Field property and lookahead technique is used to derive equations of two types of encoding/decoding schemes and their related hardware implementations**.**

A symbolic simulation based algorithm which derives optimized Boolean equations for a parameterizable data width CRC generator /checker is described in [38]. The equations are then used to generate the corresponding VHDL description, which is then synthesized to gates. The paper also presents the area and timing results of the implemented CRC circuit. The CRC-32 polynomial was implemented using the algorithm.

A methodology to determine an optimal CRC polynomial for applications using short messages is described by Tridib Chakravarty in [39]. This methodology has recognized an optimal 12-bit CRC that yields better error detection than CCITT 16-bit CRC, which is used for embedded networks having typical message lengths of 64 bits.

An exhaustive search of the 32-bit CRC design space is presented in [40]. All polynomials achieving a better HD than IEEE 802.3 CRC-32 polynomial are identified.

A theoretical result to realize high-speed hardware for parallel CRC checksums is presented in [41]. The new scheme is faster and is independent of the technology used in its realization. Here, the number of bits processed in parallel can be different from the degree of the polynomial generator. Also high-level parametric codes that are capable of generating the circuits, when only the polynomial is given, is developed.

A polynomial selection process for embedded network applications is described in [42] and a set of good general-purpose polynomials is proposed. A set of 35 new polynomials provide good performance for 3- to 16-bit CRCs for data word lengths up to 2048 bits.

Generator polynomials for CRC codes of degree eight over GF(2) are investigated by Baicheva et al. in [43]. Their minimum distance, properness and undetected error probability for binary symmetric channels (BSCs) are compared with the existing ATM standard.

A high-speed parallel CRC implementation based on unfolding, pipelining, and retiming algorithms is presented by Cheng and Parhi in [44]. The proposed design can increase the speed by 25% and control or reduce hardware implementation cost. A technique for pipelining the calculation of CRCs, such as CRC32 is introduced in [45]. It is shown how CRC throughput can scale linearly with data width and area. Also pipeline latency and operating frequency can be traded off for area.

Polynomials of degree eight over GF(2), which are used as generator polynomials for CRC codes are investigated in [46]. Their minimum distance, properness and undetected error probability for BSCs are compared with the existing ATM standard. A fast CRC algorithm that performs CRC computation for any length of message in parallel is given in [47]. First, the message is chunked into blocks of M-bits equal to the number of bits in CRC. Then CRC computation is done in parallel using Galois Field (GF) multipliers. The final CRC is obtained by accumulating the products of GF multipliers.

A circuit for CRC computation using two parallel calculation units has been implemented in a 0.35 micron process [48]. The units use 32 bits and 64 bits parallel input respectively. It can achieve I throughput higher than 5.76 Gb/s, thus indicating that 10Gb/s throughput is possible

in modern processes. A CRC calculation unit has been designed by Tomas Henriksson in [49], which handles all control symbols and alignment and the data in accordance with the specification. The unit occupies 0.51 mm2 silicon area in a 0.35 micron technology.

Nordqvist et al. [50] presents a novel architecture for CRC computation, which can be used as accelerating hardware in a protocol processor. The architecture provides high throughput and configurability for different protocols and also would reduce the workload of a host processor considerably.

Parallel computation of n-bit CRC checksum on FPGAs using logic minimization strategy is outlined in [51]. It achieves notably better performance than standard logic optimizers. A parallel fast CRC algorithm for an arbitrary length of message is presented in [52]. The algorithm first chunks the given message into blocks of fixed size equal to the degree of the generator polynomial. Then, CRC is computed in parallel for the chunked blocks using lookup tables. The results are combined using XOR operations. Simulation results show that this approach is faster and more space-efficient than previous methods.

1.8.3 Review of LDPC Error Correction codes

The empirical performance of Gallager's low density parity check codes on Gaussian channels is reported by David J.C. MacKay in [53]. It is shown the performance achieved is better than that of standard convolutional and concatenated codes. The performance achieved is almost as close to the Shannon limit similar to that of Turbo codes.

Significant improvement is shown by the analogous codes defined over finite fields GF(q) of order q>2 by in M.C. Davey and D.J.C. MacKay in [54]. The results of Monte Carlo simulations of the degree of infinite Low Density Parity Check (LDPC) codes, which can be used to attain good construction for finite codes are presented. The empirical results for the Gaussian channel of a rate ¼ code with bit error probabilities of 10^{-4} at Eb/No =.05 dB are also presented.

Low density parity-check codes known as Gallager codes, repeat-accumulate codes, and turbo codes, are reviewed by David Mackay in [55]. Results of extensive experimental studies of performance of LDPC codes, also known as “Gallager codes” [56] and “MN” (Mackay-Neal) codes [57] are presented in [58]. The results are obtained for binary symmetric channels and Gaussian channels, which demonstrate that practical performance which is better than that of standard convolutional and concatenated codes can be achieved. The performance of Gallager codes obtained is almost as close to the Shannon limit as that of turbo codes.

Turbo codes and LDPC codes are assessed in terms of their flexibility to hardware implementation by B. Levine et. al. in [59]. LDPC codes are found to be more suitable because their decoders have parallelism, the computations are easy to implement in hardware, and they are more regular than turbo decoders.

An effective general method for determining the capacity of LDPC codes using message passing decoding for any binary-input memoryless channel with discrete or continuous output alphabets is described in [60]. The capacity can be derived for any desired degree of accuracy. The general method applied to LDPC codes can also be extended to turbo codes and other concatenated coding schemes.

A joint code and decoder design is constructed for a class of (3,k) –regular LDPC codes by T. Zhang and K.K.Parhi[61]. The decoder architecture, which is partly parallel, is appropriate for efficient VLSI implementation and has very good performance.

The paper [62] presents two decoding schedules and the equivalent serialized architectures for LDPC decoders and are useful to codes with randomly generated parity-check matrices or using geometric properties of the elements in Galois fields. The staggered decoding schedule is appropriate for forward error correction applications in magnetic recording, wireless, wireline and optical communication systems.

H. Futaki and T. Ohtsuki proposed the decoding algorithm for the LDPC-COFDM(LDPC coded Orthogonal Frequency Division Multiplexing) in [63]. It used M-PSK using Gray mapping on a flat Rayleigh fading channel. LDPC-COFDM systems with M-PSK using Gray mapping have

found to have better error rate performance [64] than the systems using natural mapping on an AWGN channel. They also illustrate that, on a flat Rayleigh fading channel, the LDPC-COFDM systems with QPSK is more effective than other systems.

A 1024-b, rate-1/2, soft decision LDPC code decoder has been described by Blanksby and Howland in [65]. The decoder has a parallel architecture, supporting a maximum throughput of 1 Gb/s with 64 iterations and matches the coding gain of equivalent turbo codes. The parallel architecture enables rapid convergence resulting in a power dissipation of only 690 mW.

The paper [66] describes the improvement in Maximum Likelihood Decoding Algorithm (MLDA) proposed in [67] for the development of LDPC codes. The improved design is also applied to the decoding of Progressive-Edge-Growth (PEG) LDPC codes [68] over Binary Erasure Channels (BEC). The study demonstrates clear improvements over current LDPC decoding algorithms.

A high throughput, parallel, scalable and irregular LDPC coding and decoding system hardware is implemented on FPGA in [69]. The architecture consists twelve combinations of block lengths 648, 1296, 1944 bits and code rates 1/2, 2/3, 3/4, 5/6 based on IEEE 802.11n standard and is tested on Rice Wireless Open Access Research (WARP) Platform.

MatLab/Simulink models are developed for the Zigbee/IEEE 802.15.4 protocol in [70] and the performance evaluation is presented. The data rate and power is varied to find the effect on BER to SNR relationship. Higher the data rate, higher is the probability of error for a desired SNR. Also experiments were performed to quantify interference effect of Zigbee devices on the throughput performance of the IEEE 802.11g/WLAN and vice versa. It is found that the Zigbee interference has more effect on the IEEE 802.11g uplink rather than the downlink. Also IEEE 802.11g is greatly more affected by Bluetooth than Zigbee.

An encoder/decoder pair and code construction methodology for LDPC codes is introduced in [71] which permits the use of a wide range of code lengths and rates. The implementation was done in Virtex-4 part (XC4VLX25–12-FF668) FPGA using XST as a synthesis tool and ISE 7.1.03i. The encoder and decoder design achieved a maximum clock frequency of

278 MHz and 181 MHz respectively. Similarly the encoder design used 614 slices with 11 Block RAMs and decoder design size was 10970 slices with 46 Block- RAMs. Simulations are performed and the BER curves for an Additive White Gaussian Noise (AWGN) channel are plotted.

It was established that working in a higher order Galois field, significantly improve the performance of the LDPC code with moderate code lengths by V.S. Ganepola et.al. in [72]. Simulation studies in AWGN channel indicated that there was a significant performance gain between the codes over GF(2) , GF(4) , GF(16) , GF(64) and GF(256), reaching towards the Shannon's limit.

A method for estimating the frame error rate (FER) and bit error rate (BER) and thus the performance of LDPC codes decoded by hard-decision iterative decoding algorithms on BSCs is proposed by Hua Xiao and A. H. Banihashemi in [73]. The proposed method can be effectively used for both regular and irregular LDPC codes, a variety of hard-decision iterative decoding algorithms and also, it has a much smaller computational complexity, particularly for lower error rates compared with the conventional Monte Carlo simulation. They also proposed an algorithm in [74], which can competently find out the size and the number of the smallest error patterns that a hard-decision iterative decoder for LDPC codes over a BSC fails to correct. Thus, the error rate performance of LDPC codes over the whole range of channel crossover probabilities of interest can be estimated.

A modified min-sum decoding algorithm based on classified correction is proposed for LDPC codes by Z. Zhong et. al. in [75]. The proposed algorithm is different from the single correction in the normalized Belief Propagation (BP)-based and offset BP-based algorithms because it utilizes two corrections for minimum and sub-minimum magnitudes of input messages in check nodes. Simulation results indicate that the proposed algorithm achieves performance very close to that of the BP algorithm The decoder is implemented in VHDL and targeted on the Xilinx Virtex2p x2vp50 FPGA and achieves the maximum clock frequency of 155.8MHz.

An efficient high level approach to designing LDPC decoders is proposed in [76]. The high level design methods use Simulink, with predefined library components and with embedded Matlab codes. Performance of the LDPC decoding algorithm was evaluated by simulating the decoder over AWGN channel and plotting the BER against Signal-to-Noise-Ratio (SNR). Synthesis results for the high-level designs are compared with corresponding VHDL designs. The results were obtained using Altera's Quartus II software with Cyclone II EP2C70F672C6 FPGA device. It is found that Simulink design uses much less resources and is faster than the VHDL only design. Both designs were implemented on a Xilinx Spartan 2E FPGA.

Md. Murad Hossain et. al have introduced modified log-domain algorithm and min-sum algorithm of sum-product algorithm (SPA) for LDPC codes over GF (q) in [77]. A log-domain implementation has several advantages as far as practical implementation is concerned. The BER performance and computational complexity of the log domain algorithm, modified log-domain algorithm and modified min-sum algorithm is compared. Computer simulations verify that the modified log-domain algorithm has superior BER performance than modified min-sum algorithm for small SNR. Both modified log domain algorithm and modified min-sum algorithm requires no message multiplications. Hence they involve less computational complexity as compared to the SPA.

Yeo et al. [78] discuss architectures for LDPC decoders with methods to reduce their complexity. Area, power, and throughput constraints are of specific interest in the design of communications receivers. LDPC decoders need much less computation to achieve a similar performance, compared to turbo decoders. The choice between a serial and a parallel implementation requires the tradeoff between memory or interconnect complexity. However future practical implementations of LDPC decoders will be trading off the error correcting performance for reduced implementation complexity.

A parallel-serial, flexible, high-throughput architecture for high-performance LDPC decoder is proposed by Z. Zhang et. al. in [79]. This emulation platform can be used to capture low BER values upto 10^{-13} for a (2048,1723) RS-LDPC code and (2209,1978) array-based LDPC

code. High-order modulation formats and advanced error correcting codes are two techniques for performance improvement of ultra high-speed optical transport networks. In [80], Qi Yang et. al. present record receiver sensitivity for 107 Gb/s CO-OFDM (coherent optical OFDM) transmission through constellation expansion to 16-QAM and rate-1/2 LDPC coding.

Performance evaluation of four-dimensional nonbinary LDPC-coded modulation scheme appropriate for next-generation optical transport networks (OTNs) is presented in [81].

A novel scheme of using LDPC codes in atmospheric optical communication system is proposed by Tao Jing-jing in [82]. Receiving sensitivity is improved by employing coherent detection. The performance is evaluated by introducing atmospheric channel attenuations of 20-30 dB/km. It is found that the received power requirement is reduced by ~4 dBm at BER of 10^{-9}.

An architecture for high data rate VLF communication using Gaussian minimum shift keying (GMSK) modulation and LDPC channel coding is proposed by Arun kumar and Rajendar Bahl in [83]. The paper describes the modeling of atmospheric radio noise (ARN) that corrupts VLF signals and an algorithm for signal enhancement in presence of ARN is developed. The BER performance of the system is estimated for bit rates of 400 bps, 600 bps, and 800 bps for communication bandwidth of ~200 Hz.

A new improved construction method of LDPC code, based on the construction method of systematically constructed Gallager (SCG)(4, k) code is proposed by J. Yuan et.al. in [84]. This method has been found to save storage space and has reduced computation complexity for hardware implementation. Thereby, LDPC (5929,5624) code is constructed by the proposed construction method and has better error-correction performance, lower redundancy and lower decoding complexity than that of RS (255, 239) code and can have better suitability for optical transmission systems. Also [85] proposes novel LDPC(3969,3720) code with 6.69% redundancy and the novel LDPC(8281,7920) code with 4.56% redundancy for high speed long haul optical transmission systems and also their performance is assessed.

A study of the errors observed when an optical Gigabit Ethernet link is subject to attenuation is performed in [86]. The investigations are performed for 1000BASE-X, when the receiver power is sufficiently low, so as to induce errors in the Ethernet frames. A traffic generator is used to feed a Fast Ethernet link to an Ethernet switch, and a Gigabit Ethernet link is connected between the switch and a traffic sink and tester. A packet capture and measurement system is implemented using an enhanced driver for the SysKonnect SK-9844 NIC. A variable optical attenuator is placed in the fibre in the direction from the switch to the sink. It is found that some octets suffer from far higher probability of error than others, and that the distribution of errors varies depending on the type of packet transmitted. Similarly, in [87], it is shown that while a pseudo-random BER test may show low error rate, when the studies are performed using real network data, a (M,N) block code results in frequency components that cause non-deterministic error and a poorer overall result. The authors mention that, this conclusion is contradictory to the assumptions of a significant body of coding and protocol work. They also assert that the condition of low receiver power is increasingly likely as networks become more complex, with longer fibre lengths, optical switching systems and higher data rates.

A BER tester implementation based on the Altera Stratix II GX and IV GT development boards is described by Xiang et al. in [88]. The Stratix II GX tester operates at up to 5 Gbps and the Stratix IV GT tester operates at up to 10 Gbps, both in 4 duplex channels. The tester consists of a pseudo random bit sequence (PRBS) generator and detector, a transceiver controller, and an error logger. There is a computer interface for data acquisition and user configuration. A point-to-point serial optical link setup is developed to validate the functionality of the tester. The Stratix II GX tester was also used in a proton test on a custom designed serializer chip to record and analyse radiation-induced errors.

1.9 Organisation of the thesis

The Chapter 2 consists of the objectives of research and the methodology employed to implement the Gigabit Ethernet protocol design. The proposed implementation block diagram

and the architecture is explained in detail. Also, the evaluation techniques are summarized. Chapter 3 describes the details of the FPGA technologies based hardware implementation of the Gigabit Ethernet protocol design, the use of the command line interface and also the experimental setup developed for introducing errors in the Ethernet frames. Chapter 4 gives a background review of information theoretic concepts used in the Simulation models in this work. We review Shannon's noisy channel coding theorem, BER, PER, BER of BPSK, BSC, AWGN, CRC Algorithms, and LDPC error correction algorithms. Also, the simulation models developed in Matlab for error detection analysis and error correction analysis is described. The results are presented in Chapter 5 and the significance of the results is discussed. We also make important conclusions of the study in Chapter 5 and describe several possible avenues of future research indicated by this work.