PREFACE

This thesis focuses on the design and implementation of Gigabit Ethernet protocol tested on Altera FPGA platform to generate Gigabit Ethernet frames and study its performance. The Simulation model for Error Detection using Cyclic Redundancy Code (CRC) and Error Correction using LDPC codes in a noisy channel is developed in MATLAB 7.0, with emphasis on Gigabit Ethernet protocol. To the best of our knowledge, no such elaborate studies have been found related to the Gigabit Ethernet protocol in the past literature.

The thesis describes the designing and implementation of Gigabit Ethernet protocol testbed using FPGA platform and it's Performance Analysis. The system is designed on Altera's Stratix II GX PCI Express Development Kit using Altera's TSE (Triple Speed Ethernet) Megacore function. The throughput of Gigabit Ethernet protocol is found to be approaching 1Gbps for 9600 frame length, which is tested for different physical media. The thesis also addresses the complexities involved in the implementation of the said design.

Also a Simulation model in Matlab is developed for Error Detection using CRC code and Error Correction Analysis using LDPC codes. The Gigabit Ethernet testbed using Altera FPGA is interfaced with Matlab Simulation model, which is used to study the BER performance in a noisy Gigabit Ethernet channel. A testbed is developed for introducing optical attenuation for optic fibre channel. The results for CRC32 Error Detection algorithm for different Gigabit Ethernet frame lengths is presented. Also the results for BER performance using LDPC codes is presented for Gigabit Ethernet frame lengths of 64 , 128 and 256 bytes respectively.

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