CHAPTER 5

OPTICAL MAGNITUDE COMPARATOR (OMC) AND OPTICAL PROGRAMMABLE LOGIC CONTROLLER (OPLC)
5.1 INTRODUCTION

The previous chapters included description of LC based ESLM and their use in parallel optoelectronic logic gate formation. Besides these, there are other approaches reported in literature to implement parallel optical logic operations [1-2]. Development of various logic functional units like comparator, parity checker, encoder, decoder, adder, subtracter, etc., using such approaches are also reported [3-5]. Though the ultimate aim of these activities is to develop an optical supercomputer, many attempts have been made to enhance the speed of electronic computers using such logic functional units. While in some other reports the aim is to devise a special purpose machine that can handle restricted class of problems. The examples of these classes are image processing, pattern recognition, sorting, switching, neural network, etc. The optical implementation of these processes is demonstrated successfully by many workers [6-10]. Even fuzzy logic is implemented recently considering the decision making capability of optics[11].

In the present work the specific task of magnitude comparison is taken and is implemented optically. It is termed as Optical Magnitude Comparator (OMC). The OMC is designed and built with the intention of using it in process control applications that will be more impervious to electromagnetic interference.

Most of the optical comparators that are reported in literature are developed for image comparison/pattern matching [3,4]. Their output is specified therefore in terms of equality of two images. However in process control application, the comparators are used to know greater than, less than and equality conditions also. These three branches are important to decide the next action of control. The Optical Magnitude Comparator developed in this work is designed for this purpose. This chapter gives the design and development of OMC. Further, the design showing the use of OMC in Programmable Logic Controller (PLC) for discrete state process control is illustrated. Besides this, design of PLC using the developed optoelectronic logic gates of AND and OR is also given.
5.2 OPTICAL MAGNITUDE COMPARATOR (OMC)

In the present work 4-bit Optical Magnitude Comparator (OMC) is developed. It compares two four-bit binary, BCD or other monotonic codes and presents the three possible magnitude results at the outputs. It is optical equivalent of TTL IC 7485. The logic diagram of this IC is shown in fig. 5.1 [12]. It is implemented using the developed optoelectronic logic gates based on shadowcasting technique. The development of OMC is based on following facts.

The basic function of a comparator is to compare magnitudes of two quantities in order to determine the relationship of those quantities. In its simplest form a comparator is a device which checks the equality of two numbers. Generally Exclusive-OR gate is termed as basic comparator. Its output is logic ‘1’ if two input are not equal and logic ‘0’ if inputs are equal. Sometimes it is not only necessary to know the equality of numbers but also whether one number is greater/less/equal to the other. For example in an on/off type of heater control, controller switches the output only when the temperature crosses the setpoint. The output is on when the temperature is below the setpoint, and it is off above the setpoint. Thus in this example it is essential to know if the measured temperature is greater or less than the set temperature.

If the inputs to be compared are four-bit binary numbers represented as A and B, then they are weighted as \( A_0A_1A_2A_3 \) and \( B_0B_1B_2B_3 \) respectively. The three observations greater, less and equal are valid for each bit position in the numbers. The idea is to check for an inequality in a bit position, starting with the highest order. When such an inequality is found, the relationship of the two numbers is established and any other inequalities in lower order positions are ignored because it is possible for an opposite indication to occur—the highest order indication must take precedence.
Fig. 5.1 Logic diagram of TTL IC 7485
5.2.1 OMC system description

The block diagram of OMC is shown in fig.5.2. It consists of Operator Plane, Input Plane, Mask and Detector plane.

The operator plane consists of LEDs which are organized in group of four LEDs arranged in square matrix form. The switching configurations of these LEDs are fixed for obtaining particular operation. These operations are performed on input binary pattern.

The input binary patterns are obtained by spatially encoding and superimposing the two binary inputs according to rules of shadowcasting and then fed to ESLM as described in section 3.3.3[b] of chapter three. This is done by the controller which is attached to the ESLM as shown in fig.5.2. For the developed OMC, ESLM consists of two kinds of inputs, primary inputs and secondary/derived inputs. The primary inputs are the two numbers which are weighted four bit binary inputs. The secondary inputs are attained because, shadowcasting technique operates on two binary inputs. Thus if logic operation is to be performed on more than two binary inputs then first it is performed on two of them. Then it is performed on the resultant of the first two and the third input and so on. The intermediate output which is observed in this process is called secondary/derived output which acts as an input for the next logic operation. Also from fig. 5.1 it is seen that sometimes it is necessary to get combination of two inputs by certain logic operation and then it is combined with another input by using some different logic operation. The intermediated outputs obtained in this process which further act like input are also termed as secondary/derived inputs. For these reasons, a feedback loop is seen from output plane to input plane which provides the secondary outputs as inputs for OMC.

The output shadowgram obtained due the logic operator is filtered out using mask and only the intensity at the middle square is allowed to fall on photodetectors placed at output plane. The photodetectors which sense the secondary outputs are connected to ESLM through controller unit. These outputs which are fed back to input are spatially encoded to give secondary inputs. These derived inputs then combine with other derived or primary inputs to give the final result. The output is observed at three terminals which are indicated by numbers 1,2,3. Depending on the
Fig. 5.2 Block diagram of the developed OMC
state of light in these terminals whether the word A is greater, less than or equal to word B is decided. A truth table shown in Table 5.1 helps to take decision.

5.2.2 Performance test

The comparison of two weighted binary numbers A and B using OMC is demonstrated. These two numbers are as follows

\[
\begin{array}{cccc}
A_3 & A_2 & A_1 & A_0 \\
B_3 & B_2 & B_1 & B_0 \\
\end{array}
\]

\[
\begin{array}{cccc}
A & 0 & 1 & 0 & 0 \\
B & 0 & 0 & 0 & 0 \\
\end{array}
\]

Figure 5.3 shows the detailed schematic diagram for the implementation of the same. \(A_3, A_2, A_1, A_0, B_3, B_2, B_1, B_0, A_3 \oplus B_3, A_2 \oplus B_2, A_1 \oplus B_1\) and \(A_0 \oplus B_0\) are the primary inputs. As shown in this figure, these are given as inputs to planes P2 and P3. In addition to these inputs, secondary inputs are derived from detector plane and fed to these planes. They contain input pattern in spatially encoded form as given by shadowcasting method. This is done by the controller attached to these planes. These two planes which are placed in front of the other give the superimposition of two input planes. Presently instead of two input planes, only one is used by directly filling the superimposed spatially encoded pattern. This plane is made of the developed LC based ESLM. The controller unit is attached to it to fill the required input pattern. The blocks in this controller are shown in fig.5.4. The controller consists of BAM and ENCODE, the program for encoding and superimposition of the input numbers. The output of ENCODE is given as input to CSG block in BAM which is discussed in section 3.3.3 [b]. The secondary outputs detected by photodetectors are fed to ENCODE through Digital In channel of SYSTEM 570. From here they go to CSG as in the case of primary inputs and then ESLM is filled with primary as well as secondary inputs. Here PC is used in the demonstration of OMC which acts as CSG as well pattern encoder for the simplicity. However it is possible to use hard wired circuit for both the purposes. The operator plane P1 performs logic operation on these inputs to give final result. As shown in figure 5.3, it consists of LEDs arranged in group of four in the square form. The LEDs shown by black circles indicate off state and LEDs shown by transparent circle indicate on state. The result obtained
# Table 5.1
## Truth-table for OMC

<table>
<thead>
<tr>
<th>Comparing Inputs</th>
<th>Cascading Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A3,B3 A2,B2 A1,B1 A0,B0</td>
<td>IA&gt;B IA&lt;B IA=B</td>
<td>1 2 3</td>
</tr>
<tr>
<td>A3&gt;B3 X X X</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3&lt;B3 X X X</td>
<td>X X X</td>
<td>L H L</td>
</tr>
<tr>
<td>A3=B3 A2&gt;B2 X X</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2&lt;B2 X X</td>
<td>X X X</td>
<td>L H L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1&gt;B1 X</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1&lt;B1 X</td>
<td>X X X</td>
<td>L H L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0&gt;B0</td>
<td>X X X</td>
<td>H L L</td>
</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0&lt;B0</td>
<td>X X X</td>
<td>L H L</td>
</tr>
<tr>
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<td>X X X</td>
<td>L H L</td>
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<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
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<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
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</tr>
<tr>
<td>A3=B3 A2=B2 A1=B1 A0=B0</td>
<td>X X X</td>
<td>L H L</td>
</tr>
</tbody>
</table>
Primary Inputs

Encoder

CSG

PISO Shift register

SIPO Shift register

LCD drivers

32

ESLM

Photodetector Array

Secondary Inputs

System 570

RNG

LCD Drivers

BAM

Fig. 5.4 Controller for input plane in OMC
for the comparison of given two binary numbers is shown in photograph 5.1. From the figure, following result is obtained

Terminal 1 - Presence of light
Terminal 2 - Absence of light
Terminal 3 - Absence of light

When the obtained output is compared with the Table 5.1 the number A is found to be greater than number B which is the correct result. Here, the detector circuit is made such that presence of light gives 5V and the absence of light gives 0.9V at the output of photodetector. Light intensities corresponding to 5V and 0.9V represent logic ‘1’ and logic ‘0’ level respectively.

5.2.3 Demonstration of OMC in indexing application

The use of the developed OMC is demonstrated in position indexing application. In this demonstration, out of two inputs of OMC, one indicates reference position and the other as current position. A mask is made on which the positions are recorded in 4-bit binary form as shown in fig.5.5. The size of each square in the mask is 1mm X 1mm. Light is allowed to fall on this mask, from one side. This mask is moved with a X-Y positioner which moves the mask by 1mm in each step. As the mask moves, the light coming through it is detected by 4-photodetectors which are placed on the other side of the mask. These photodetectors represent the current position of the mask. This is given as one input to OMC. The other input is reference position. The experimental setup of this assembly is shown in fig.5.6. The developed OMC compares current position, with the reference one. According to table 5.1, the output observed at terminals indicates whether current position is greater/less/equal to the reference position. In this demonstration reference position, is given in encoded form is 1000. Positions of mask at locations 0111, 1000, 1001 are compared with the reference position. The obtained result is shown in photograph-5.2.
Photograph 5.1 Comparison of two binary numbers using OMC
Fig. 5.5 Position encoding
Fig. 5.6 OMC in position indexing
Photograph 5.2 Comparison of different positions of the mask with reference position
5.2.4 Results and Discussion

The Optical Magnitude Comparator consisting of 32 gates is designed and implemented successfully[13]. The gates used in OMC are based on shadowcasting method. These gates operate in SIMD architecture. The advantage is that logic operations can be done on many inputs with one LED set. As a result it is not necessary to have number of LED sets equal to number of inputs when same type of logic operations are to be done on many inputs.

The developed OMC has three output terminals. The presence of light at terminal 1 indicates A>B and 2 gives A<B result. While giving the result A=B at terminal 3, condition of the expansion inputs IA>B, IA<B and IA=B which act as 5th input bit positions, are checked. They are the least significant bit positions and are used to cascade many such magnitude comparators. Thus the result of number A to be equal to B is determined from the least significant bit positions.

There are reports of developing optical comparator in literature [3,4]. In the approach of Guilfoyle et. al. it seen that optical comparator is designed for comparing two words[3]. The design proposes use of detector as OR gates. It shows whether two words are equal or not. The optical comparator developed by Jing Chen et. al shows the comparison of binary images [4]. In this approach also the output indicates whether two images are equal or not. In this method the comparator uses parallel optical logic gates with electronic feedback. Similar approach is adapted in this work for development of OMC. In both the approaches suggested earlier the comparison merely gives the equality of two numbers. While the approach used in this work for development of OMC provides three possible magnitude results since it is analog of TTL IC 7485. This type of OMC may be useful in the control application where the controlling action depends on whether set value is less than, greater than or equal to reference value. Another reason for proposing the OMC in control application is its optical implementation which give advantages of parallelism and electromagnetic interference immunity. The OMC makes use of ESLM as input data plane. The electronic control used in it imparts dynamic behavior to the SLMs. Considering this the OMC is proposed in on-line control application[14].

In the following section design of a Programmable Logic Controller using
developed OMC and optoelectronic logic gates is given.

5.3 OPTICAL PROGRAMMABLE LOGIC CONTROLLER (OPLC)

The solution to the problem of how to control discrete state process control is to use computer based device called programmable logic controller (PLC). They are designed to perform repetitive or sequential industrial processes[15]. The basic PLC configuration consists of four parts, the central processing unit(CPU), the input/output sections(I/O) and the programming device[16]. To design these four blocks the event sequence is given for the process under control. Once it is finalized, the system hardware and process controller is symbolically and schematically represented by ladder diagram. Conventionally the basic symbols for ladder diagram are contacts and coils. It is used to create controller’s operational program. The main purpose is to control outputs based on input conditions. These conditions are set by logic gates such as AND, OR or combinatorial logic function like comparison. In the planned OPLC the developed OMC and optoelectronic logic gates are proposed for implementing these logic conditions. It was thought that instead of using conventional PLC, if optics is incorporated a good isolation between input and output is possible. With high degree of isolation transient noise immunity to prevent false triggering or retransmission of noise may be achieved. PLC design for two processes, filling the tank with liquid, energizing solenoid valves is described below.

5.3.1 Design of OPLC

In the planned OPLC the basic symbols for ladder diagram are designed in terms of logic operator and/or ESLMs. Thus there is an optical layer inbetween input and output module which gives the logic conditions for the given set of input and output. This is shown in fig.5.7.

In the present work the design of PLC for two processes is given. In one type the logic conditions to get particular output for given set of inputs are given by optoelectronic AND and OR logic gates. In other type alongwith these logic operations, a comparator action is involved to implement the rungs. In this process
Fig. 5.7 Blocks in OPLC
these compare conditions are designed using the developed OMC. The two processes A and B which are designed using optoelectronic logic gates and OMC are described below.

5.3.2 Process A with Optoelectronic logic gates only

Consider an example of filling tank with liquid, heating it to specified temperature and keep their for 30 minutes. This process consists of following event sequence

1. Fill tank with liquid,
2. Heat and stir liquid to temperature set point and hold for 30 minutes,
3. Empty the tank,
4. Repeat from step 1,

As mentioned earlier, after finalizing the event sequence, the system hardware and process controller is symbolically and schematically represented by ladder diagram. The ladder diagram for the described event is shown in fig. 5.8. All the six rungs are designed using the optoelectronic logic gates which are described in section 4.2 as follows

As shown in figure 5.8 rung R1 contains two switches start and stop. When normally open push-button switch (Start) is depressed, the control relay CR1 is energized. Now its normally open contact closes bypassing stop switch so that the relay stays closed. Thus it is latched. This rung is designed using optoelectronic logic gates in following way

The primary operation is of starting the process and latching it till stop button is depressed. The start condition and latching of coil in process A is designed as shown in fig. 5.9(a). The output of start is connected to ESLM1. Initially the start button is not pressed and stop button is closed. In this situation the output coil CR1 is not energized. The condition of start is denoted by ESLM1, coil CR1 is indicated by ESLM2 and that of stop button by ESLM3. The ESLMs used in this design are T type. The ESLM1 and ESLM2 are arranged to perform logic OR operation and
Fig. 5.8 Ladder diagram of Process A (Conventional method)
ESLM3 is placed to give AND operation with the resultant of OR gate. The unpressed start button and unenergized coil CR1 gives logic ‘0’ input data to ESLM1 and ESLM2. The closed stop button gives logic ‘1’ input data to ESLM3. In this condition incident light is blocked and photodetector placed at output plane cannot observe any light. Thus the coil CR1 which is driven by the output of photodetector will remain unenergized. As soon as the start button is depressed, the ESLM1 will momentarily get logic ‘1’ input data so that the output of ‘(ESLM1 + ESLM2) AND ESLM3’ will be logic ‘1’. As per the developed optoelectronic logic gates presence of light indicates logic ‘1’. Thus photodetector will receive light for this combination and coil CR1 will be energized. Figure 5.9(a) represents R1 using the optoelectronic logic gates giving the following conditions.

(Start switch unpressed OR CR1 unenergized) AND stop switch closed then CR1 is unenergized.

(Start switch depressed OR CR1 unenergized) AND stop switch closed then CR1 is energized.

(Start switch open OR CR1 energized) AND stop switch closed then CR1 is energized.

This gives the start and latch condition in rung R1.

As depicted in figure 5.8 the rung R2 opens input valve provided the output valve is not open, until full level is not reached. This means the input valve is kept energized until the tank is full. During this time output valve should remain close.

The following condition is performed in rung R2.

CR1 energized AND L closed AND Vout closed then Vin is energized.

The design for this stage is shown in fig. 5.9(b). The condition of CR1 is symbolized by ESLM4, that of level switch by ESLM5 and Vout by ESLM6. The ANDing of data in ESLM4, ESLM5 and ESLM6 is done by putting these ESLMs one in front of the
Fig. 5.9(a) Rung R1 using OPLC (Process A)
Fig. 5.9(b) Rung R2 using OPLC (Process A)
other. When CR1 is energized ESLM4 will receive logic ‘1’ data, if level switch is closed ESLM5 will get logic ‘1’ data and if Vout is closed ESLM6 will attain logic ‘1’ data. In this state the input valve Vin will be opened and liquid will start flowing in the tank.

The R3 is used for turning on the stirrer provided output valve is not open. This condition is

\[ Vin \text{ closed AND } Vout \text{ closed then start the stirrer} \]

Design for implementing this condition is shown in fig. 5.9(c). The condition of Vin is indicated by ESLM7 and that of Vout by ESLM8. Similar to the previous step ANDing is achieved by putting these ESLMs one in front of the other. If true condition i.e. presence of light is observed at output the stirrer(S) will start.

The rung R4 starts 30 minutes timer.

When Vin is closed timer TR1 is started. This is achieved by getting the condition of Vin in ESLM9.

The heater is controlled by R5. This rung is energized as temperature goes above and below the limit. When the timer TR1 times out, the rung is de-energized when CR1 is closed, Vin is closed and timer TR1 is closed and the temperature switch HI is closed then heater H is will be made on. Here the temperature switch proposed is NOTC type i.e. it is normally open and after set temperature is reached it closes. Thus temperature of heater is maintained around set value. The design for this event is shown in fig.5.9(d) and can be described as follows

\[ CR1 \text{ is closed AND Vin is closed AND TR1 is closed AND HI is closed then heater is made on.} \]

\[ CR1 \text{ is closed AND Vin is closed AND TR1 is closed AND HI is open then heater is made off.} \]

This is achieved by ANDing the data from CR1, Vin, TR1 and HI. The data
Fig. 5.9(c) Rung R3 using OPLC (Process A)
Fig. 5.9(d) Rung R5 using OPLC (Process A)
indicating the state of these units is fed in ESLM9, ESLM10, ESLM11 and ESLM12 respectively. Whenever the output of AND is bright light the photodiode drives the heater coil and makes it on otherwise the heater is made off.

R6 is energized to open the output valve provided input valve is open. Output valve remains open until empty limit switch opens.

Finally after 30 minutes TR1 opens. If TR1 is open, L is open the Vout is opened provided Vin is closed. The design for this shown in fig.5.9(e).

\[ TR_1 \text{ is open AND } L \text{ is open AND } Vin \text{ closed then Vout is opened.} \]

The process repeats itself starting from first step until the stop switch is opened. When stop switch is pushed to open, the output of AND in the first step is 0 and the process is reset.

\[ (\text{Start switch depressed OR CR1 unenergized}) \text{ AND stop switch open then CR1 is unenergized.} \]

The ladder diagram for OPLC is shown in fig.5.10. As seen from this figure, the ladder consists of rungs which are set by ESLMs performing optoelectronic AND, OR logic operation. The input module supplies inputs to ESLMs. These inputs decide the transparency of ESLMs and either transmit or block incident light which is detected by photodetector. The coils in the output unit of conventional PLC are replaced by photodiode which further drives the output devices such as input/output valve, stirrer and heater.

5.3.3 Process B with optoelectronic logic gates and OMC

This process is of energizing three solenoid valves. These solenoid valves indicated by S1, S2, S3 are energized after certain time delay. The event sequence for this process is

1. After the start button is pushed and latched by coil CR1, solenoid S1 is energized 5 seconds later,
Fig. 5.9(e) Rung R6 using OPLC (Process A)
Fig. 5.10 Ladder diagram for OPLC (Process A)
2. 10 seconds later solenoid S2 is energized,
3. At preset time solenoid S3 is energized,
4. All the three solenoids will remain on until the circuit is reset by opening start contact,

After finalizing the event sequence, the system hardware and process controller is symbolically and schematically represented by ladder diagram. This ladder diagram is shown in fig. 5.11.

As shown in this ladder diagram, rung R1 sets the start and latch condition. When the start button is pushed, it energizes output coil CR1 and seals its contact. This latches the coil CR1. This rung is designed in the same fashion as that of rung R1 of process A.

The condition of start is denoted by ESLM1. The condition of coil CR1 is indicated by ESLM2 and that of stop button by ESLM3. The unpressed start button and unenergized coil CR1 gives logic ‘0’ data to ESLM1 and ESLM2. The closed stop button gives logic ‘1’ data to ESLM3. As mentioned in R1 of process A, the output coil CR1 will be unenergized initially and after start button is pushed it will remain in latch. The designed start and latch condition is shown in fig. 5.12(a). It executes following event

(Start switch unpressed OR CR1 unenergized) AND stop switch closed then CR1 is unenergized.

(Start switch depressed OR CR1 unenergized) AND stop switch closed then CR1 is energized.

(Start switch open OR CR1 energized) AND stop switch closed then CR1 is energized.

The rung R3 in conventional PLC is used for comparing the accumulated time with the reference time. When CR1 is energized, the on-delay timer T1 starts. This timer has a preset time of 20s. The accumulated time is stored in register of
Fig. 5.11 Ladder diagram of Process B (Conventional method)
Fig. 5.12(a) Rung R1 using OPLC (Process B)
programming device. A reference time of 5 s is stored in one memory location. The reference time of 5 s is compared with the accumulating time. Solenoid S1 stays energized as the timer advances beyond the accumulated count of 5 s because of less than compare command in rung R3.

The compare condition used in this rung is designed using the developed OMC. In this case two inputs to the OMC can be reference time corresponding to 5 s and the accumulated time. The accumulated time varies from 1 s to 20 s. Thus only after 5 s, the reference time will become equal to or less than accumulated time. Less than or equal to condition will be given by the developed OMC and accordingly the solenoid S1 will be energized. ESLM4 is used to display superimposed reference time of 5 s and accumulated time. Also it contains derived inputs as mentioned earlier. The plane P1 is the operator plane indicating the operation of magnitude comparison. Less than or equal to condition obtained in this rung can be detected at three output terminals 1, 2 and 3. When the required condition is detected by three photodetectors at the output, the solenoid S1 will be energized. The designing of R3 using OMC is shown in fig.5.12(b). Its result is as follows

Reference time \textbf{COMP} Accumulated time

\text{reference time} \leq \text{accumulated time} \text{ then energize solenoid S1.}

Here COMP represents magnitude comparison using OMC.

Rung R4 will energize solenoid S2 and will retain this condition until the stop button is pressed. This condition will be obtained as shown in fig.5.12(c). In this design reference time is changed to 10 s and is compared with the accumulated time in the same way as described in R3 to energize solenoid S2.

\text{reference time} \leq \text{accumulated time} \text{ then energize solenoid S2}

Rung R5 shows that after 20 s, the timer reaches its preset value and solenoid S3 is energized. All three solenoids will remain on until the program is reset by opening the stop switch.
Fig. 5.12(b) Rung R3 using OPLC (Process B)
Fig. 5.12(c) Rung R4 using OPLC (Process B)
In the design of this step, when timer T1 reaches its preset value, ESLM6 will get input data of logic ‘1’ which will turn solenoid S3 on. This condition is shown in fig. 5.12(d).

This process continues till it is reset by stop switch. The ladder diagram of process B using OPLC is shown in fig. 5.13. As in case the of process A, the output devices are activated by photodetector.

5.3.4 Discussion

PLC is used for controlling discrete state processes which are described by particular sequence of events through which process accomplishes some objective. The answers to these events are in True or False form. Always the controlling action is decided by true or false outputs set by an event or combination of them. This helps to build a logic in a sequential manner. This is called as ladder logic where each rung in the ladder describes the interdependence of events logically. In conventional PLC the ladder logic is built by contacts of switches and coils.

In the present work design is made to replace the electronic logic in each rung by optoelectronic logic gates and OMC. The normally open and normally close contacts are used to represent the status of input in conventional logic. Here these are replaced by ESLMs which can have transparent state or dark state. Here, the ESLM with transparent state is termed as normally close and that with dark state as normally open switch.

The designed OPLC uses optoelectronic logic gates which are described in section 4.2. The reason is the simplicity involved in their implementation. However to form the compare condition the developed OMC is used which makes use of optical gates implemented with shadowcasting technique.

5.4 CONCLUSION

Optical logic offers several advantages and this would be the technology of future. In this work logic gates are demonstrated using the developed LC based ESLMs. As an attempt of furthering this activity a combinatorial logic function, the
Fig. 5.12(d) Rung R5 using OPLC (Process B)
Fig. 5.13 Ladder diagram for OPLC (Process B)
Optical Magnitude Comparator consisting of 32 gates was chosen and implemented successfully. The developed OMC presently compares two four bit binary words. It makes use of liquid crystal based ESLMs as data plane. The electronic control over ESLM imparts dynamic nature to the system. Therefore the use of it is proposed in process control application which is a time based concept. In this work the design of programmable logic controller is given using the developed logic gates and OMC. The PLCs are used in discrete state process control application. In this technique first the ladder is formed which gives the sequence of execution of discrete events included in the process. This is symbolically represented by a ladder diagram. Each rung in this ladder diagram represents a logic condition necessary for the particular event. In conventional PLC the positions of the switches determine the logic AND, OR or comparator operation. In the design of Optical Programmable Logic Controller the proposal is made to derive these logic conditions using optoelectronic logic gates and OMC.

Optoelectronic devices like optoisolators, optotriac are being used in process control field to give good electric isolation between input and output. On the similar line it was thought that the optoelectronic logic gates/combinatorial circuits which found use in image processing, pattern recognition, signal processing application [7-9] would be advantageous in process control area. The designed OPLC may give better electric isolation between input and output and reduced noise. Also grounding and impedance mismatch problems will be alleviated because of use of optoelectronic logic functions.

In the present work, either a single input is considered or it is in the form of one-dimensional array. The real advantage of OMC or OPLC would be for processing two-dimensional input array simultaneously.

As the ESLM used in this work is based on LC there is a limitation on speed but with some good materials such as ferroelectric liquid crystals speed can be increased. Further improvement in the performance would come when the interconnects and feedback would be provided optically using optical fibers/waveguides instead of present electrical wiring. None the less here a working demonstration of a optical logic system is provided. This by far is a new development which has potential to grow further mainly in process control field.
REFERENCES


